MANIPAL SCHOOL OF INFORMATION SCIENCES
MANIPAL
(A constituent unit of MAHE, Manipal)

INDEX

DIRECTOR
MANIPAL SCHOOL OF INFORMATION SCIENCES
MAHE, MANIPAL - 576 104

Deputy Registrar - Academics (Tech.)
MANIPAL ACADEMY OF HIGHER EDUCATION
MANIPAL - 576 104

REGISTRAR
MANIPAL ACADEMY OF HIGHER EDUCATION
MANIPAL

MANIPAL

ACADEMY *of* HIGHER EDUCATION

(Institution of Eminence Deemed to be University)

Master of Engineering - ME (VLSI Design)

Syllabus

July 2024 Onwards

MANIPAL SCHOOL OF INFORMATION SCIENCES
MANIPAL ACADEMY OF HIGHER EDUCATION
MANIPAL - 576104.KARNATAKA. INDIA.

Program Educational Objectives / Outcomes (PEOs)

PEO 1: Successfully engage in challenging careers with professional approach in the areas of analog and digital VLSI design and related domains of engineering.

PEO 2: Demonstrate competence in identifying and analysing technical problems, suggest feasible and innovative solutions using their core competence in VLSI design and thereby support the technological growth of the nation.

PEO 3: Impart quality technical education, engage in research and contribute to knowledge creation and sharing.

PEO 4: Possess analytical, communicative and leadership skills, and demonstrate the ability to work in multidisciplinary and multi-cultural environments.

PEO 5: Be self-motivated and remain continuously employable by engaging in lifelong learning.

Program Objectives / Outcomes (POs)

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program.

PO4: An ability to demonstrate knowledge of underlying principles and evaluation methods for integrated circuit technology.

PO5: An ability to use modern tools for engineering design problems, analyze the performance and optimize the systems-level approaches.

Program Structure

ME (VLSI Design) - I Semester									
Course Code	Course Name	No. of Hrs./week				Duration of Exam in Hrs	Maximum Marks		
		Lecture	Tutorial	Practical	Credit		Internal 50	External 50	Total 100
VLS 5001	High Level Digital Design	3	-	-	3	3	50	50	100
VLS 5101	Data Structures	3	-	-	3	3	50	50	100
VLS 5102	Digital Systems and VLSI Design	3	-	-	3	3	50	50	100
VLS 5103	Verification	3	-	-	3	3	50	50	100
	Elective - I	3	-	-	3	3	50	50	100
VLS 5051	High Level Digital Design Lab	-	-	3	1	3	50	50	100
VLS 5151	Data Structures Lab	-	-	3	1	3	50	50	100
VLS 5152	Digital Systems and VLSI Design Lab	-	-	3	1	3	50	50	100
VLS 5153	Verification Lab	-	-	3	1	3	50	50	100
	Elective - I Lab	-	-	3	1	3	50	50	100
MPT 5100	Mini Project - I	-	-	-	4	-	100	-	100
PSD 5100	Professional Skill Development - I	-	-	-	1	-	100	-	100
Total		15	-	15	25				

ME (VLSI Design) - II Semester									
Course Code	Course Name	No. of Hrs. / week				Duration of Exam in Hrs	Maximum Marks		
		Lecture	Tutorial	Practical	Credit		Internal 50	External 50	Total 100
VLS 5201	Advanced VLSI Design	3	-	-	3	3	50	50	100
VLS 5202	Low Power VLSI Design	3	-	-	3	3	50	50	100
VLS 5203	Scripting for VLSI	3	-	-	3	3	50	50	100
VLS 5204	Universal Verification Methodology	3	-	-	3	3	50	50	100
	Elective - II	3	-	-	3	3	50	50	100
VLS 5251	Advanced VLSI Design Lab	-	-	3	1	3	50	50	100
VLS 5252	Low Power VLSI Design Lab	-	-	3	1	3	50	50	100
VLS 5253	Scripting for VLSI Lab	-	-	3	1	3	50	50	100
VLS 5254	Universal Verification Methodology Lab	-	-	3	1	3	50	50	100
	Elective - II Lab	-	-	3	1	3	50	50	100
MPT 5200	Mini Project - II	-	-	-	4	-	100	-	100
PSD 5200	Professional Skill Development - II	-	-	-	1	-	100	-	100
TOTAL		15	-	15	25				

ME (VLSI Design) -III & IV Semesters									
VLS 6098	Project Work	-	-	-	25				
Total Number of Credits to Award Degree							75		

List of Electives (Theory)

Elective - I		Elective - II	
Course Code	**Course Name**	**Course Code**	**Course Name**
VLS 5131	CAD for VLSI	VLS 5231	Advanced Logic Synthesis
VLS 5132	System on Chip Design	VLS 5233	Machine Learning for VLSI Design
ESD 5001	Digital Signal Processing	VLS 5234	Physical Design
MVT 5101	VLSI Fabrication Technology	ENP 5230	Entrepreneurship
		ESD 5232	IT Project Management

List of Electives (Lab)

Elective - I		Elective - II	
Course Code	**Course Name**	**Course Code**	**Course Name**
VLS 5181	CAD for VLSI Lab	VLS 5281	Advanced Logic Synthesis Lab
VLS 5182	System on Chip Design Lab	VLS 5283	Machine Learning for VLSI Design Lab
ESD 5051	Digital Signal Processing Lab	VLS 5284	Physical Design Lab
MVT 5151	VLSI Fabrication Technology Lab	ENP 5280	Entrepreneurship Lab
		ESD 5282	IT Project Management Lab

SEMESTER I

VLS 5001: High Level Digital Design	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Apply combination logic gates and arithmetic circuits
2. Analyze data path functional units and optimization
3. Analyze sequential logic and finite state machine circuits with timing aspect
4. Apply Field Programming Gate Arrays and First In First Out

Analyze AMBA bus architecture

Unit	Topics	No. of Hours
I	Introduction: Digital System; VLSI design Flow Digital System Design: https://onlinecourses.nptel.ac.in/noc21_ee39/	2
II	Combinational Design: Number System: Binary; 1's Complement; 2's Complement. Single Precision, Double precision	1
III	Arithmetic Circuits: Ripple Carry, Carry Look-Ahead, Carry Skip, Carry Increment, Tree Adder: Brent Kung, Sklansky, Kogge Stone Adder	2
IV	Datapath Functional Units: Comparator; Funnel Shifter, Multi Input Adder; Multiplier; Divider.	2
V	Optimization: logic optimization techniques, Branch method, Petrick Methods	3
VI	Sequential Design: Latch; Flip-flops; scan Flip-flop; Registers Set; Design of counters	2
VII	FSM: Mealy Machine; Moore Machine; Mixed Machine, FSM optimization	4
VIII	Timing Analysis: Foundry Library; Liberty format; Gates: Propagation Delays; Flops: Propagation Delay; Setup time; hold Time; contamination delay; Recovery time; Removal time; Clock frequency; Jitter; Skew (source & network latency); Timing Paths; Multi-input path; Clock Budget; Multi-Clock; Multi-Cycle Path; False Path; Retiming with examples (Intel FPGA)	6
IX	Introduction to FPGA: PLD; FPGA design flow	2
X	FPGA: Introduction to FPGA Boards with examples (Intel FPGA)	4
XI	Digital Design Application: FIFO Design-1; FIFO Design-2 [SNUG Papers]	4

XII	AMBA Bus Specification: AHB; APB	4

References

1. https://onlinecourses.nptel.ac.in/noc21_ee39
2. "An Engineering Approach to Digital Design", Flectcher
3. "Rapid Prototyping of Digital Systems - SOPC Edition", James O Hamblen, Tyson S Hall, Michael D Furman
4. "Simulation and Synthesis Techniques for Asynchronous FIFO Design", Clifford E. Cummings [SNUG Paper]
5. "Simulation and Synthesis Techniques for Asynchronous FIFO Design with Asynchronous Pointer Comparisons", Clifford E Cummings, Peter Alfke [SNUG Paper]

ARM Specification2.0

VLS 5101: Data Structures	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Design programs for implementation of linked lists, stack and queues.
2. Design programs for implementation of binary search tree, sorting and searching, dictionary and Hash Table
3. Design programs for graphs and shortest path techniques.

Unit	Topics	No. of Hours
I	Programming Fundamentals - (https://www.coursera.org/learn/programming-fundamentals) **Algorithm specification and analysis techniques:** Analysis of recursive programs. Solving recurrence equations. General solution for a large class of recurrences.	3
II	**Elementary data structures:** Implementation of Array, lists, stacks, queues, Trees	17
III	**Sorting & Searching:** Bubble, selection, insertion, Quick sort, heap sort, merge sort. Linear search and binary search.	6
IV	**Hash Tables and Graph:** Hashing and Dictionaries. Representation of graphs. Depth First Searching. Breadth First Searching, Minimum cost spanning tree. Single source shortest paths and all-pairs shortest path	10

References

1. "Data Structures& Algorithms" Aho, Hopcroft and Ulmann
2. "Data structures and algorithm analysis in C", Mark Allen Weiss
3. "Computer Algorithms", Ellis Horowitz, Sartaj Sahni, Sanguthevar Rajasekaran
4. "Introduction to Algorithms"- Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest. MIT Press.

VLS 5102: Digital Systems and VLSI Design	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Explain various CMOS process technologies and manufacturing issues.
2. Analyze the static and dynamic behavior of MOSFETs and the secondary effects of the MOS transistor model.
3. Design and test CMOS combinational and sequential logic at transistor level, including mask layout.
4. Describe circuit characterization and manufacturing issues.

Units	Topics	No. of Hours
I	MOS transistor theory: (https://in.coursera.org/learn/semiconductor-1) Ideal I-V Characteristics, C-V Characteristics, CMOS inverter - DC Characteristics, Noise Margin, Static load MOS inverters, NELS, NELT, HMOS, Pass transistor, Transmission gate, tristate inverter, MOSFET Models, Non-ideal I-V effects.	10
II	CMOS circuit and layout design: Combinational and Sequential Circuit Design, Basic physical design of simple gates, CMOS logic structures (Dynamic CMOS Logic, C2MOS Logic, CMOS and NP Domino	4
III	Circuit characterization: Resistance estimation, Capacitance estimation, delay time calculation, principles of modelling the gate, Switching characteristics, CMOS gate transistor sizing, Power dissipation, Scaling principles	7
IV	**CMOS Subsystem Design:** Data path operations - Adder, Comparator, Counter, Semiconductor memory elements - SRAM, DRAM	5
V	**CMOS Technologies:** Wafer Formation, Photolithography, Well and Channel Formation, Silicon Dioxide (SiO2), Oxidation, Isolation Gate Oxide, Gate and Source/Drain Formations, Contacts and Metallization, Passivation, SOI.	6
VI	**Layout Design Rules:** Design Rule Background, Micron and Lambda Design Rules	3
VII	**Manufacturing Issues:** Antenna Rules, Layer Density Rules, Resolution Enhancement Rules.	1

References

1. "CMOS digital integrated circuits analysis and design", Kang Sung Mo and Leblebici Yusuf, McGraw Hill, 1999.

2. "Principles of CMOS VLSI Design: A systems perspective", 2nd Edition, Neil H. E. Weste, Kamran Eshraghian, Addison Wesley, 1999.
3. "CMOS VLSI Design: A circuits & systems perspective", 3rd Edition, Neil H. E. Weste, David Harris, Addison Wesley, 2007.
4. "Microchip Fabrication", by Peter Van Zant, 5th Edition, McGraw-Hill, International Edition.

VLS 5103: Verification	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Apply verification challenges and types of verification for digital systems
2. Analyze verification planning and assertions
3. Apply testbench infrastructure
4. Evaluate stimulus response
5. Apply coverage driven verification and post silicon validation

Unit	Topics	No. of Hours
I	**Introduction:** Verification Challenges, Productivity, Design for Verification, Methodology	2
II	**Types of Verifications & Approaches:** Formal Verification, Property Based Verification, Functional Verification, Rule Checking-Linting, Black Box Verification, White Box Verification, Grey Box Verification	3
III	**Verification Planning:** Planning Process, Response Checking Verilog and System Verilog Design Techniques: https://www.coursera.org/learn/fpga-hardware-description-languages	2
IV	**Assertions:** Specifying Assertions, Assertions on Internal DUT Signals, Assertions on External Interfaces, Assertion Coding Guidelines, Reusable Assertion-Based, Qualification of Assertions	5
V	**Assertions Examples:** Immediate assertion with ALU design and priority encoder designs, Concurrent Assertions with Counters, FSM, Memory and FIFO using Overlapped and non-overlapped implication operators with bind operator	6
VI	**Assertions for Formal Tools:** Model Checking and Assertions, Assertions on Data	2
VII	**Test bench Infrastructure:** Testbench Architecture, Simulation Control, Data and Transactions, Transactors, Transaction-Level Interfaces, Timing Interface, Callback Methods, Ad-Hoc Testbenches, Legacy Bus-Functional Model	8
VIII	**Stimulus and Response:** Generating Stimulus, Controlling Random Generation, Self-Checking Structures	4

IX	**Coverage-Driven Verification:** Coverage Metrics, Coverage Models, Functional Coverage Implementation, Feedback Mechanisms.	3
X	**Post-Silicon SoC Validation:** Introduction, Validation Activities, Planning for Post-Silicon Readiness, Post-Silicon Debug Infrastructure, Generation of Tests, Post-Silicon Debug	1

References

1. https://www.coursera.org/learn/fpga-hardware-description-languages
2. Janick Bergeron, Verification methodology manual for SystemVerilog, Springer.
3. Janick Bergeron, Writing Testbenches using System Verilog, Springer.
4. William K. Lam, Hardware Design Verification - Simulation and Formal Method Based Approaches.
5. Pallab Dasgupta, A Roadmap for Formal Property Verification, Springer

ELECTIVES - SEMESTER I

VLS 5131: CAD for VLSI	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Explain various VLSI design flows, design methods and technologies.
2. Describe various VLSI design steps and relevant design automation tools, Explain types of synthesis, Illustrate design representations and graph-based problem formulations.
3. Illustrate and apply CAD algorithms used in VLSI design automation.

Unit	Topics	No. of Hours
I	**Introduction to VLSI Design Methodologies:** The VLSI deign problem, Design domains, Design Actions, Design methods and technologies	6
II	**Review of VLSI Design Automation Tools:** Quick tour of design automation tools for various methods and levels of VLSI design, Physical Design, Verification, Design Management	8
III	**High Level Synthesis:** Introduction to Synthesis, Design representations and transformations	3
IV	**High Level Synthesis Algorithms:** Partitioning, Scheduling, Allocation algorithms	10
V	**Floor Planning and Placement:** Floor planning concepts, Shape Functions and Floor plan sizing, Placement, Types of placement problems and algorithms https://in.coursera.org/learn/vlsi-cad-layout#about	3

VI	**Routing:** Local routing, Types of local routing problems, Area and Channel routing problems and algorithms, Global routing https://ict.iitk.ac.in/courses/vlsi-physical-design/	3
VII	**Layout Compaction:** Design rules, symbolic layout, Algorithms for layout compaction.	3

References

1. "Graph theory" , Narsingh Deo (Prentice-Hall of India private ltd)
2. "Graph theory" , Gibbons
3. "Algorithms for VLSI Design Automation" ,Sabih H. Gerez (John Wiley and Sons)
4. "High Level Synthesis -Introduction to chip and System Design" , Daniel Gajski, Nikil Dutt, Allen Wu, Steve Lin (Kluwer Academic Publishers)
5. "Logic synthesis and verification algorithms" , Gary D. Hachtel, Fabio Somenzi (Kluwer Academic Publishers)
6. "Computer aided logical design with emphasis on VLSI " , Frederick J Hill, Gerald R. Peterson (john Wiley & sons)

VLS 5132: System on Chip Design	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Apply electronic system level flow for system on chip design
2. Analyze robust processors and memory
3. Apply hardware interconnects, interfaces and applications

Unit	Topics	No. of Hours
I	**Introduction to System Approach:** System Architecture overview, Components of the System, Introducing Hardware/Software Codesign, The Driving Factors of Hardware/Software Design, The Hardware-Software Codesign space.	3
II	**Electronic System Level Flow:** Specification and Modeling, Pre-Partitioning Analysis, Partitioning, Post-Partitioning Analysis and Debug, Post-Partitioning Verification, Hardware Implementation, Software Implementation.	4
III	**Design Principles in SOC Architecture:** Heterogeneous & Distributed Data Processing, Heterogeneous & Distributed Data Communications, Heterogeneous & Distributed Data Storage, Hierarchical Control.	3

IV	**Processors:** Introduction to Processors, Processor Selection for SOC, Basic Concepts in Processor Architecture, RISC Pipeline, Basic Concepts in Processor Microarchitecture, Basic Elements in Instruction Handling, Buffers, Branches, Robust Processors	6
V	**Memory Design:** Introduction, Overview of SOC Internal and External Memories, Scratchpads and Cache Memory, Cache Organization, Cache Data, Write Policies, Strategies for Line Replacement at Miss Time, Other Types of Caches, Split I- and D-Caches and the Effect of Code Density, Multilevel Caches, Virtual-to-Real Translation, SOC (On-Die) Memory Systems, Board-Based (Off-Die) Memory systems, Simple DRAM and the Memory Array, Models of Simple Processor-Memory Interaction. Introduction to Embedded Systems Software and Development Environments: https://www.coursera.org/lecture/introduction-embedded-systems/2-memory-architectures-4C3Jo	6
VI	**Hardware Interconnects:** Introduction, Overview of Interconnect Architectures, Bus Architecture, SOC Standard Buses, Analytic Bus Models, Beyond the Bus (NOC with Switch Interconnects), Some NOC Switch Examples, Layered Architecture and Network Interface Unit, Evaluating Interconnect Networks.	4
VII	**Hardware/Software Interfaces:** Introduction, Synchronization Schemes, Memory-Mapped Interfaces, Coprocessor Interfaces, Custom-Instruction Interfaces.	3
VIII	**Application Studies:** 3-D Graphics Processor / Software Defined Radio with 802.16, Universal Serial Bus	7

References

1. https://www.coursera.org/lecture/introduction-embedded-systems/2-memory-architectures-4C3Jo
2. Michael J. Flynn , Wayne Luk, "Computer System Design System-On-Chip", John Wiley & Sons, Inc., Publication, 2011.
3. Brain Bailey, Grant Martin, Andrew Piziali, "ESL Design and Verification: A Prescription for Electronic System-Level Methodology", Morgan Kaufmann Publication, 2007.
4. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Codesign", Springer, 2010.
5. Don Anderson, USB System Architecture (USB 2.0), Mindshare, Inc., 2001.

ESD 5001: Digital Signal Processing	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Analyze Fast Fourier Transform (FFT) algorithms on computational complexity.
2. Design IIR and FIR filters using various sampling techniques.
3. Interpret Multirate Signal Processing and Adaptive Filters.
4. Infer architecture, memory management and pipelining concepts of General and TMS320C67XX Digital Signal Processor.

Unit	Topics	No. of Hours
I	**Review: (Self Study):** Introduction Classification of signals and systems, brief discussions on z-transform, inverse z-transform & Fourier transform, DFT, linear convolution using circular convolution & DFT	
II	**FFT Algorithms:** Radix-2 DIT-FFT Algorithm, DIF-FFT Algorithm. Assignments (Problems).	3
III	**Filter Structures:** IIR Filter Structure - Direct Form I & II, CSOS, PSOS & Transpose structures - FIR Filter Structures - Direct Form, Cascade form, Linear Phase Filter structures, Assignments (Problems). (MOOC: Digital Signal Processing Introduction https://nptel.ac.in/courses/117102060)	5
IV	**Design of FIR filters:** Using Frequency Sampling & Windows - Assignments (Problems).	5
V	**Design of IIR Filters:** Butterworth & Chebychev filters design using impulse invariance & bilinear transformation techniques, Design of IIR filter using pole placement technique. Assignments (Problems).	7
VI	**Multirate Signal Processing:** Decimation, Interpolation, Sampling rate conversion by a rational factor, structures, Polyphase filter structures, Time variant Filter structure, Application of Multirate signal processing to Phase Shifter, Subband coding of Speech signal, Digital Filter Bank Implementation, QMF Filter bank	10
VII	**Adaptive Filters:** Class of Optimal Filters - Predictive Configuration, Filter Configuration, Concept of adaptive noise cancellation, Noise Canceller Configuration. LMS adaptive Algorithm, Application of LMS algorithm to the optimal filter configurations. Adaptive noise canceller as a high-pass filter	3

VIII	**DSP Processor:** Introduction to PDSPs - Multiplier and Multiplier Accumulator (MAC), Modified Bus structures and memory access schemes, Multiple access memory, Multiported Memory, VLIW architecture, Pipelining, Special Addressing modes, On-chip Peripherals. TMS320C6711 DSP processor: Architecture, Instruction set and assembly language programming	3

References

1. Sanjith K Mitra, "Digital Signal Processing", McGraw Hill Education, 4th Edition, July 2013.
2. Oppenheim and Schafer, "Digital Signal Processing", Pearson, First Edition, 1975.
3. Roman Kuc, "Digital Signal Processing", McGraw-Hill Education, 1988.
4. Proakis and Manolakis, "Digital Signal Processing", Prentice - Hall, Inc., Third Edition, 1996.
5. Rabinder and Gold, "Theory and Application of Digital Signal Processing", Prentice Hall India Learning Private Limited, 1988.
6. Hwei P Hsu, Schaum's Outline of "Signals and Systems", 3rd Edition, 2013.
7. Symon Haykins, "Signals and Systems", Wiley, Second Edition, 2002.

MVT 5101: VLSI Fabrication Technology	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Apply microelectronic fabrication, clean room technology, and process of crystal growth
2. Apply lithography and oxidation processes in fabrication technology
3. Apply diffusion, ion implantation, thin film deposition to develop integrated circuits

Unit	Topics	No. of Hours
I	**Introduction:** Microelectronic Fabrication - A Historical Perspective and Basic concepts, An Overview of Monolithic Fabrication Processes and Structures, Metal-Oxide-Semiconductor (MOS) Processes, Basic NMOS Process, Basic Complementary MOS (CMOS) Process, Basic Bipolar Processing MOOC: Fundamentals of electronic device fabrication, https://onlinecourses.nptel.ac.in/noc21_mm26/preview	5
II	**Cleanroom technology:** Clean Factories, Wafer cleaning, Gettering, Manufacturing methods and equipment, Measurement methods, Models and simulation, Future trends	4
III	**Crystal Growth:** Physics of the Crystal growth, wafer fabrication and basic properties of silicon, wafers	2

IV	**Lithography:** The Photolithographic Process, Photomask Fabrication, Comparison between positive and negative photoresists, Exposure Systems, Characteristics of Exposure Systems, E-beam, Lithography, X- ray lithography	7
V	**Oxidation:** Growth mechanism and kinetic oxidation, oxidation n techniques and systems, oxide properties, oxide induced defects, characterization of oxide films, Use of thermal oxide and CVD oxide; growth and properties of dry and wet oxide, dopant distribution, oxide quality	6
VI	**Diffusion and Ion Implantation:** The Diffusion Process, Mathematical Model for Diffusion, Constant-, The Diffusion Coefficient, Successive Diffusions, Diffusion Systems, Implantation Technology, Mathematical Model for Ion Implantation, Selective Implantation, Channelling, Lattice Damage and Annealing, Shallow Implantations	7
VII	**Thin film deposition, contacts, packaging and yield:** Chemical Vapor Deposition, Physical Vapor Deposition, Epitaxy, Metal Interconnections and Contact Technology, Silicide and Multilayer-Contact Technology, Copper Interconnects and Damascene Processes, Wafer Thinning and Die Separation, Die Attachment, Wire Bonding, Packages, Yield.	7

References

1. https://onlinecourses.nptel.ac.in/noc21_mm26/preview
2. Peter Van Zant, Microchip Fabrication, 5th Edition, MC-Graw Hill International Edition
3. S.M. Sze, VLSI technology, Tata McGraw-Hill, Second Edition, 2017.
4. R.C. Jaeger, Introduction to microelectronic fabrication, Prentice Hall, Second Edition, 2013.
5. Silicon VLSI Technology Fundamentals, Practice and Modelling By James D. Plummer · 2009

VLS 5051: High Level Digital Design Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Implement combination logic gates and arithmetic circuits using Verilog
2. Implement sequential logic and finite state machine circuits with timing aspect using SystemVerilog
3. Design data path functional units and optimize for given specification using SystemVerilog
4. Implement Memory Blocks, Simple Processor, Enhanced Processor using Intel FPGAs
5. Implement Algorithms in Hardware, Basic Digital Signal Processing using Intel FPGAs

Unit	Topics	No. of Hours
I	Design and Simulation of combinational circuits: Number System: Binary; 1's Complement; 2's Complement, Ripple Carry, Carry Look-Ahead Adder	6

II	Design and Simulation of sequential circuits: Latch; Flip-flops; scan Flip-flop Registers Set; Design of counters, Mealy Machine; Moore Machine; Mixed Machine	6
III	Design and Simulation of Datapath Functional Units and advanced Digital Systems: Comparator; Funnel Shifter, Multi Input Adder, Multiplier; Divider, FIFO Design	9
IV	Design and simulate with Intel FPGA: Memory Blocks, Simple Processor, Enhanced Processor, Implement Algorithms in Hardware, Basic Digital Signal Processing	15

References

1. Sutherland, S., et al. "SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling, vol. 2." (2006).
2. SystemVerilog 3.1a Language Reference Manual

VLS 5151: Data Structures Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Analyze recursive programs, solve a general class of recurrence relations.
2. Design programs for implementation of linked lists, stack, queues, binary search tree, sorting and searching.
3. Design programs for sorting and searching.
4. Design programs for dictionary, hash tables, graphs and shortest path techniques.

Unit	Topics	No. of Hours
I	**Algorithm specification and analysis techniques:** Analysis of recursive programs. Solving recurrence equations. General solution for a large class of recurrences.	3
II	**Elementary data structures:** Implementation of Array, lists, stacks, queues, Trees	18
III	**Sorting & Searching:** Bubble, selection, insertion sort, Quick sort, heap sort, merge sort. Linear search and binary search.	6
IV	**Hash Tables and Graph:** Implement Hashing and Dictionaries, graphs. Depth First Searching. Breadth First Search, Minimum cost spanning tree. Single source shortest paths.	9

References

1. Introduction to Algorithms - Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest. MIT Press.
2. Data Structures and Algorithms - Aho, Hopcroft and Ulmann. Pearson Publishers.

VLS 5152: Digital Systems and VLSI Design Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Design and simulate simple combinational and sequential circuits
2. Draw layout of simple digital circuits, carryout DRC and LVS
3. Understand VLSI design process and fabrication technology
4. To provide experience designing integrated circuits using Computer Aided Design (CAD) Tools

Unit	Topics	No. of Hours
I	**MOS transistor theory, CMOS circuit:** I-V Characteristics of NMOS, PMOS, CMOS inverter - DC characteristics, Transfer Characteristics, Noise Margin, Pass transistor, Transmission gate, tristate inverter, Design and simulation of simple Combinational and Sequential Circuits, CMOS logic structures (Dynamic CMOS Logic, C2MOS Logic, CMOS and NP Domino Logic) **Circuit characterization and CMOS Subsystem Design:** Resistance estimation, Capacitance estimation, delay time calculation, principles of modelling the gate, Switching characteristics, CMOS gate transistor sizing, Power dissipation. Data path operations - Adder, Comparator, Counter, Semiconductor memory elements - SRAM, DRAM	20
II	Basic physical design of simple gates, combinational and sequential circuits DRC, LVS	10
III	Study of CMOS Fabrication Technologies, Manufacturing Issues	6

References

1. "CMOS digital integrated circuits analysis and design", Kang Sung Mo and Leblebici Yusuf, McGraw Hill, 1999.
2. "Principles of CMOS VLSI Design: A systems perspective", 2nd Edition, Neil H. E. Weste, Kamran Eshraghian, Addison Wesley, 1999.
3. "CMOS VLSI Design: A circuits & systems perspective", 3rd Edition, Neil H. E. Weste, David Harris, Addison Wesley, 2007.
4. Cadence User manual.

VLS 5153: Verification Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Apply verification for combinational circuits with direct and random test vectors using Verilog
2. Apply verification for sequential logic circuits using SystemVerilog constructs
3. Create verification environment for data path functional units using SystemVerilog constructs
4. Create verification environment for memory blocks, simple processor using SystemVerilog constructs
5. Apply concurrent and immediate assertions using SystemVerilog constructs

Unit	Topics	No. of Hours
I	Simulate and verify combinational circuits: Number System: Binary; 1's Complement; 2's Complement. Single Precision, Double precision, Ripple Carry, Carry Look-Ahead adder	9
II	Simulate and verify sequential circuits: Latch; Flip-flops; scan Flip-flop; Registers Set; Design of counters, Mealy Machine; Moore Machine; Mixed Machine	6
III	Construct verification environment for the verification of Datapath Functional Units: Comparator; Funnel Shifter, Multi Input Adder; Multiplier; Divider, FIFO Design	6
IV	Construct and verify immediate assertion: ALU design and priority encoder designs, Concurrent Assertions with Counters, FSM, Memory and FIFO using Overlapped and non-overlapped implication operators with bind operator	15

References

1. Spear, Chris. SystemVerilog for verification: a guide to learning the testbench language features. Springer Science & Business Media, 2008.
2. SystemVerilog 3.1a Language Reference Manual

VLS 5181: CAD for VLSI Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Experiment data structures for design representations using graphs.
2. Develop programs to implement high level synthesis algorithms.
3. Develop programs to implement physical design algorithms.

Unit	Topics	No. of Hours
I	Introduction to Synthesis, Design representations and transformations	9
II	High level synthesis algorithms	18

III	Physical design algorithms	9

References

1. "Graph theory", Narsingh Deo (Prentice-Hall of India private ltd)
2. "Algorithms for VLSI Design Automation", Sabih H. Gerez (John Wiley and Sons)
3. "High Level Synthesis -Introduction to chip and System Design", Daniel Gajski, Nikil Dutt, Allen Wu, Steve Lin (Kluwer Academic Publishers)

VLS 5182: System on Chip Design Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Apply design space exploration for system on chip design
2. Create data path & control path components and memory
3. Analyze channels, mutex, semaphore, FIFO

Unit	Topics	No. of Hours
I	Partitioning, Post-Partitioning Analysis and Debug, Post-Partitioning Verification, Hardware Implementation, Software Implementation.	7
II	Design of various SOC Architecture - Heterogeneous & Distributed Data Processing, Heterogeneous & Distributed Data Communications, Heterogeneous & Distributed Data Storage, Hierarchical Control.	10
III	Design and simulation of simple Processors	6
IV	Design and simulation of Memory - Simple DRAM and the Memory Array, Models of Simple Processor-Memory Interaction	6
V	Study of 3-D Graphics Processor / Software Defined Radio with 802.16, Universal Serial Bus	7

References

1. Michael J. Flynn, Wayne Luk, "Computer System Design System-On-Chip", John Wiley & Sons, Inc., Publication, 2011.
2. Brain Bailey, Grant Martin, Andrew Piziali, "ESL Design and Verification: A Prescription for Electronic System-Level Methodology", Morgan Kaufmann Publication, 2007.
3. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Codesign", Springer, 2010.
4. Don Anderson, USB System Architecture (USB 2.0), Mindshare, Inc., 2001.

ESD 5051: Digital Signal Processing Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Analyse Fast Fourier Transform (FFT) algorithms on computational complexity.
2. Describe the structures for IIR and FIR filters.
3. Interpret Multirate Signal Processing and Adaptive Filters.

Unit	Topics	No. of Hours
I	To get acquainted with the use of MATLAB software tool	6
II	Design and analysis of various filter structures using MATLAB - FIR filters, IIR filters, Adaptive filters	21
III	Study and use of DSP processors - TMS320C6711 DSP processes.	9

References

1. Sanjith K Mitra, "Digital Signal Processing", McGraw Hill Education, 4th Edition, July 2013.
2. Oppenheim and Schafer, "Digital Signal Processing", Pearson, First Edition, 1975.
3. Roman Kuc, "Digital Signal Processing", McGraw-Hill Education, 1988.
4. Proakis and Manolakis, "Digital Signal Processing", Prentice - Hall, Inc., Third Edition, 1996.
5. Rabinder and Gold, "Theory and Application of Digital Signal Processing", Prentice Hall India Learning Private Limited, 1988.
6. Hwei P Hsu, Schaum's Outline of "Signals and Systems", 3rd Edition, 2013.
7. Symon Haykins, "Signals and Systems", Wiley, Second Edition, 2002.

MVT 5151: VLSI Fabrication Technology Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Apply semiconductor technology parameters using computer aided design support during process development
2. Apply lithography and oxidation processes in fabrication technology
3. Apply diffusion, ion implantation, thin film deposition to develop integrated circuits

Unit	Topics	No. of Hours
I	Apply semiconductor device models to describe the device behaviour	9
II	Design approaches for developing semiconductor process technologies	9
III	Analyze the device behaviour of diodes and transistors (bipolar and MOSFETs) and extract SPICE parameters necessary for circuit simulation	18

References

1. Peter Van Zant, Microchip Fabrication, 5th Edition, MC-Graw Hill International Edition

2. S.M. Sze, VLSI technology, Tata McGraw-Hill, Second Edition, 2017.
3. Silicon VLSI Technology Fundamentals, Practice and Modelling By James D. Plummer · 2009

MPT 5100: Mini Project - I	L	T	P	C	Total hours
	0	0	0	4	48

Course Outcome:

1. Identify the real-world and socially relevant problems and perform feasibility analysis for finding solutions.
2. Organize work effectively as a member in a team, examine, experiment, and communicate technical information constructively.
3. Develop and implement solutions to the identified problems by applying research methodology and development life cycle with appropriate documentation by incorporating ethical standards.

Unit	Topics	No. of Hours
I	Problem identification, literature survey, formation of detailed specifications.	48
II	Design and implementation of the proposed system architecture.	
III	Demonstrate an ability to present and defend project work carried out to a panel of experts.	

References

1. Research articles and Online Resources.

PSD 5100: Professional Skill Development - I	L	T	P	C	Total hours
	0	0	0	1	12

Course Outcome:

1. Identify and synthesize important themes in the field of engineering which transform socio-economic ecosystem.
2. Develop competence to communicate effectively in oral and written forms.
3. Effective management of time, involve in reflective learning and adhere to the professional code of conduct.

Unit	Topics	No. of Hours
I	Report writing involves identifying the topic of interest from current issues in the domain of engineering and technology or inter disciplinary domains, then framing the order in the report, writing abstract,	12

	deciding on the content itself, conclusion and future scope of the topic and properly citing the references from bibliography.	
II	Presenting in classroom to audience where content spoken, the conceptual knowledge and presentation skills (like audibility, eye contact, memory) of speaker is assessed.	

References

1. Research articles and Online Resources.

SEMESTER II

VLS 5201: Advanced VLSI Design	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Analyze and model analog circuits
2. Design analog and mixed signal CMOS analog integrated circuits
3. Apply the methods learned in the class to design and implement practical projects

Unit	Topics	No. of Hours
I	CMOS passive elements: (https://in.coursera.org/learn/electronics) Resistor: Fabrication-Different layers used, Layout techniques and practical considerations, Temperature and voltage dependence resistors, Active resistors - advantages, Capacitor: Fabrication - "poly-substrate", "poly-poly", "metal-poly" - comparison, Layout techniques, Temperature and voltage dependence, Active Capacitors.	3
II	**Analog MOSFET Models:** Low frequency MOSFET Model: Small-signal model of the MOSFET in saturation, Derivation for g_m and r_0 High frequency MOSFET Model: Variation of transconductance with frequency	1
III	**Current Sources and Sinks:** Current Source, current Sink and Current Mirror - Differences, Applications ,Current Mirror-Basic current mirror, The cascode current mirror - advantages, derivation ,for o/p resistance r0,Layout of current Sources/Sinks/Mirrors, Matching in MOSFET mirrors, Other Current Sources /Sinks/Mirrors- Wilson current mirror, Regulated cascode current mirror	3

IV	**References:** Voltage Dividers, Sensitivity and Fractional temperature coefficients-Resistor-MOSFET divider, MOSFET-only voltage divider, Current Source Self-Biasing-Threshold voltage referenced self-biasing, Diode referenced self-biasing, Thermal voltage referenced self-biasing, Bandgap voltage references, Bandgap referenced biasing, Beta Multiplier Referenced Self-Biasing-A voltage reference, Operation in the Sub-threshold region	4
V	**CMOS Single Stage Amplifiers:** Amplification - need for amplification, basic concepts, Important performance parameters - "Analog Design Octagon" ,Common Source (CS) Amplifier-Derivation for Av and comparison of CS Amplifier with: Passive resistor load, MOSFET/Diode-Connected/ /Active load, Current source load - Common Drain Amplifier (or Source Follower)-Derivation for Av and comparison of CD Amplifier with: Passive resistor load, MOSFET/Diode-Connected/ /Active load, Current source load - Common Gate Amplifier-Derivation for Av and comparison of CG Amplifier with: Passive resistor load, MOSFET/Diode-Connected/ /Active load, Current source load - The Push-Pull Amplifier, Noise and Distortion in Amplifiers-A class AB Amplifier - Modeling Amplifier Noise	6
VI	**Differential Amplifiers:** The Source Coupled Pair- Current Source Load, Common-Mode Rejection Ratio, Noise, Matching Considerations. The Source Cross-Coupled Pair-Current Source Load Cascode Loads, Wide-Swing Differential Amplifiers, Current Differential Amplifier, Constant Transconductance Diff-Amp.	4
VII	**Frequency Response of Amplifiers:** Introduction, Frequency response of single stage amplifiers, Frequency response of Differential pair.	3
VIII	**Noise:** Statistical characteristics of noise, types of noise, representation of noise in circuits, noise in single-stage amplifiers, noise in differential pairs, noise bandwidth.	3
IX	**Operational Amplifiers:** Basic CMOS Op-Amp Design-Characterizing the op-Amp, Compensating the Op-amp Without Buffer, The Cascode Input Op-amp, Operational Transconductance Amplifiers.	2

X	**Nonlinear Analog Circuits:** Design of Basic CMOS Comparator, Characterizing the Comparator Adaptive Biasing, Analog Multipliers- The Multiplying Quad, Level Shifting, Multiplier Design Using Squaring Circuits.	2
XI	**Dynamic Analog Circuits:** The MOSFET Switch - Switched-Capacitor Integrator Circuits	2
XII	**Data Converter Fundamentals and Architectures:** Sample-and-Hold (S\H) Characteristics, DAC and ADC Specifications, Architectures - Cyclic DAC, Pipeline DAC, Pipeline ADC, Integrating ADCs, SAR ADC	3

References

1. "CMOS Circuit Design, Layout, and Simulation", Baker, Li, & Boyce, IEEE Press, 1998.
2. "Design of Analog CMOS Integrated Circuits", Razavi, McGraw-Hill, Inc., 2000.
3. "Analog Integrated Circuit Design ", Johns & Martin, John Wiley & Sons, 1997.
4. "CMOS Analog Design, 2nd Ed", Allen & Holberg, Oxford Univ. Press, 1987.
5. "Analysis and Design of Analog Integrated Circuits ", Gray & Meyer, John Wiley & Sons, 1984.
6. "Analog VLSI", Mohammed Ismail, & Terri Fiez, McGraw-Hill, Inc.
7. "VLSI - Design Techniques for Analog and Digital Circuits", Geiger, Allen, & Strader McGraw-Hill, Inc.,
8. Recent papers from IEEE Journal of Solid state Circuits and other technical magazines

VLS 5202: Low Power VLSI Design	**L**	**T**	**P**	**C**	**Total hours**
	3	**0**	**0**	**3**	**36**

Course Outcome:

1. Describe various components of power in CMOS VLSI Design.
2. Comprehend various leakage power reduction techniques, technology and scaling related aspects of low power VLSI design.
3. Explain dynamic power reduction techniques and system level issues.

Unit	Topics	No. of Hours
I	**Introduction to Low Power Design**	2
II	Overview of power dissipation in CMOS: Dynamic and Static power components, Leakage current components, Factors affecting leakage power, Examples https://nptel.ac.in/courses/106105034	5

III	**Circuit techniques for leakage power reduction:** Stacking - natural and artificial, Multiple V_{th} techniques - Multiple Channel Doping's, Multiple Oxide CMOS (MOXCMOS) Circuits, Multiple Channel Lengths, Multiple Body Biases, Multi-threshold-voltage CMOS (MTCMOS), Dual Threshold CMOS, Variable Threshold CMOS (VTMOS), Dynamic Threshold CMOS (DTMOS), Dynamic V_{th} techniques - V_{th} hopping scheme, Dynamic voltage scaling (DVTS) scheme. https://nptel.ac.in/courses/106105034	8
IV	**Technology scaling for dynamic power reduction:** Scaling techniques - constant voltage, constant field and lateral scaling. **Voltage scaling approaches:** Reliability-Driven Voltage Scaling, Technology-Driven Voltage Scaling, Energy x Delay Minimum Based Voltage Scaling, Voltage Scaling through Optimal Transistor Sizing, Voltage Scaling using Threshold Reduction, Architecture-Driven Voltage Scaling.	8
V	**Glitch power:** Generated and propagated glitches, Glitch power analysis, Reduction techniques, Gate triggering approach.	3
VI	**Clock gating:** Principle, Combinational and sequential clock gating, Clock gating efficiency.	2
VII	Adiabatic techniques for low power	2
IX	Logic optimization for low power, Power modelling, Power analysis	2
X	System level issues in multi-voltage designs, Level shifters	2
XI	Low power design of building blocks	2

References

1. "Low-Power CMOS VLSI Circuit Design", Kaushik Roy and Sharat C. Prasad, Wiley-Interscience.
2. "CMOS Low Power Digital Design", A. Chandrakasan & R. Brodersen, Kluwer Academic Pubs. 1995.
3. "Low Power Design Methodologies", J. Rabaey & M. Pedram, , Kluwer Academic Pubs. 1996.
4. "Low - Power Digital VLSI Design, Circuits and Systems", Bellaour & M.I. Elamstry ,Kluwer Academic Publishers, 1996.
5. S. Imam & M. Pedram, Kluwer Academic Publishers, 1998.
6. "Logic synthesis for Low - power VLSI Designs", B.G.K.Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998.
7. "Power Aware Design Methodologies", Pedram, Massoud, Rabaey, Jan M., Kluwer Academic Publishers.
8. "Low-power Digital Systems Based on Adiabatic- Switching Principles", W.C. Athas, L. Swensson, J.G. Koller and E. Chou, , IEEE Transactions on VLSI Systems, vol. 2, pp. 398-407, December 1994.

9. "A survey of power estimation techniques in VLSI circuits", F. Najm, IEEE Transactions on VLSI Systems, vol. 2, pp. 446-455, December 1994.

VLS 5203 Scripting for VLSI	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Discover shell script programmatically using different features and debugging the code.
2. Apply SED & AWK commands to do more complex task in easy way.
3. Apply PERL scripts that create and change scalar, array and hash variables.

Unit	Topics	No. of Hours
I	Linux Fundamentals: Operating System , kernel, Shell , File system, Process, Network.	2
II	Version Control: git	1
III	Shell scripting : Variables, Arithmetic, Quotes, Redirection, pipe, filters, Wild cards , exit status Command line arguments, constructs	4
IV	Power Utilities: Cut , paste , tr, uniq Sed, Grep , Awk , Regular expressions and Make	7
V	Perl : variables, constructs, pattern matching, File handling	3
VI	Tcl/Tk : variables, Datatypes, constructs, Widgets	4
VII	Python: Data types, List, Tuples, Dictionary, Constructs , OOPS , File handling	11
VII	UML : Building blocks , Modelling Types	2
IX	Design Patterns : Design Pattern, why design pattern , Design pattern in Python	2

References

1. https://archive.nptel.ac.in/courses/106/105/106105161/
2. Neil H. E. Weste, David Harris, Kamran Eshraghian, "Principles of CMOS VLSI Design: A systems perspective", Third Edition, Addison Wesley,2008
3. Majid Sarrafzadeh, C. K. Wong , "An introduction to VLSI physical design", McGraw Hill, 1996, ISBN 0070571945, 9780070571945, 334 pages
4. Khosrow Golshan, "Physical design essentials: an ASIC design implementation perspective", Springer, 2007, ISBN 0387366423, 9780387366425, 211 pages
5. Ban P. Wong, Anurag Mittal, Yu Cao, Greg Starr Contributor Ban P. Wong, Anurag Mittal, Yu Cao, "Nano-CMOS circuit and physical design", John Wiley and Sons, 2004, ISBN 0471466107, 9780471466109

VLS 5204: Universal Verification Methodology	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Apply UVM library basic using Object Oriented Programming
2. Apply Interface and automate UVC Creation
3. Apply configuration & Factory and UVM Callbacks
4. Apply testbench integration and stimulus generation
5. Apply Register Abstraction Layer TLM and Communications

Unit	Topics	No. of Hours
I	UVM overview: Verification Planning and Coverage-Driven Verification, Multi-Language and Methodologies. UVM Testbench and environments, Interface UVCs, System and Module UVCs, the System Verilog UVM class library	2
II	Object Oriented Programming: Introduction, What is an object in OOP, Distributed development environment, Classes, Objects, Programs, Using generalization and inheritance, polymorphism in OOP, Downcast, Class libraries, Static methods and attributes, parameterized classes, packages and namespaces. Programming In Modern C++: https://onlinecourses.nptel.ac.in/noc22_cs103/	3
III	UVM library basics: Using UVM library, Library Base Classes, the uvm_object class, the uvm_component class, UVM configuration mechanism, TLM in UVM, UVM factory, UVM message facilities, callbacks.	2
IV	Interface UVCs: Stimulus modeling and generation, creating the driver, creating the sequencer, connecting the driver and sequencer	5
V	Automating UVC Creation: Creating the collector and monitor, modeling topology with UVM, creating the Agent, creating the UVM verification component, creating UVM sequences, configuring the sequencer's default sequence, coordinating end-of-test, implementing protocol-specific coverage and checks, handling reset, packaging interface UVCs	3
VI	Component Configuration and Factory: Establish and Query Component Parent-Child Relationships, Set Up Component Virtual SystemVerilog Interfaces with uvm_config_db, Constructing Components and Transactions with UVM Factory, Implement Tests to Configure Components, Implement Tests to Override Components with Modified Behavior	3
VII	UVM Callback: Create User Callback Hooks in Component Methods, Implement Error Injection with User Defined Callbacks, Implement Component Functional Coverage with User Defined Callbacks, Review Default Callbacks in UVM Base Class.	2

VIII	Simple Testbench integration: Testbenches and Tests, creating a simple testbench, testbench configuration, creating a test, creating meaningful tests, virtual sequencers and sequences, checking for DUT correctness, implementing a coverage model.	4
IX	Stimulus generation topics: Fine control sequence generation, executing multiple sequences concurrently, using p_sequencer, using pre_body() and post_body() methods, controlling the arbitration of items, interrupt sequences, protocol layering.	2
X	Register Abstraction Layer: Registers, Specification, Adapter, Integrating, Integration, Register Model Overview, Model Structure, Quirky Registers, Model Coverage, Back Door Access, Generation, Stimulus Abstraction, Memory Stimulus, Sequence Examples, Built in Sequences, Scoreboarding, Functional Coverage.	4
XI	System UVCs and Testbench Integration: Introduction, module and system UVC architecture, sub-components of module and system UVCs, module UVC configuration, the testbench, sequences, coverage, stand-In mode, scalability concerns in system verification, module UVC Directory structure.	3
XII	TLM Communications: TLM Push, Pull and Fifo Modes, TLM Analysis Ports, TLM Pass-Through Ports, TLM 2.0 Blocking and Non-Blocking Transport Sockets	3

References

1. https://onlinecourses.nptel.ac.in/noc22_cs103/
2. Sharon Rosenberg, Kathleen Meade, "A Practical Guide to Adopting the Universal Verification Methodology (UVM)", Lulu publishers, 2010.
3. Vanessa R. Cooper, "Getting started with UVM: A beginner's guide", Verilab publisher, 2013.
4. UVM Cookbook, Verification Academy, 2013.
5. UVM User's guide, Accellera, 2011.

ELECTIVES - SEMESTER II

VLS 5231: Advanced Logic Synthesis	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Apply logic synthesis process.
2. Analyze procedure involved in logic synthesis of combinational and sequential circuits.
3. Apply multilevel logic synthesis and technology mapping.

Unit	Topics	No. of Hours
I	Introduction to logic synthesis	1
II	**Two-level logic synthesis:** Introduction, Boolean algebra concepts, Minimization using k-map, Minimization using Tabular method, Consensus theorem, Iterative Consensus theorem , Recursive computation, Unate covering problem a) Reduction technique b) MIS algorithm c) Branch and bound algorithm https://www.coursera.org/learn/vlsi-cad-logic#about	14
III	**Sequential logic synthesis:** Introduction, Basics of FSM concept, Minimization of completely specified FSM, Equivalent partition algorithm, Minimization of Incompletely specified FSM, Compatible table, Maximum compatibles, Prime compatibles, Binate covering problem, FSM traversal algorithms, Depth first search, Breadth first search, Shortest path, State encoding and optimization	13
IV	**Multilevel logic synthesis:** Introduction, Algebraic and Boolean Division, Kernels and Cokernels Algebraic and Boolean re-substitution methods	5
V	**Technology mapping:** Graph covering and Technology mapping, Tree covering by Dynamic programming, Decomposition, Delay optimization and Graph covering	3

References

1. "Logic Synthesis and Verification Algorithms", Gary D. Hachtel and Fabio Somenzi (Kluwer Academic Publishers)
2. "Logic Minimization Algorithms For VLSI Synthesis", Robert K. Brayton ,Gary D. Hachtel, Curtis T. McMullen and Alberto L. Sangiovanni-Vincentelli (Kluwer Academic Publishers)

VLS 5233: Machine Learning for VLSI Design	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Apply goals, applications, types and design issues of machine learning techniques.
2. Analyze different machine learning algorithms.
3. Apply machine learning in VLSI computer-aided design.

Unit	Topics	No. of Hours
I	**Introduction:** Aims and applications of machine learning, learning systems, various aspects of developing a learning system	3
II	**Linear and Logistic Regression:** Linear regression, Decision trees, overfitting	3

III	**Instance based learning:** Instance based learning, Feature reduction, Collaborative filtering-based recommendation	3
IV	**Bayesian learning:** Probability and Bayes learning	3
V	**Logistic Regression:** Logistic Regression, Support Vector Machine, Kernel function and Kernel SVM	3
VI	**Neural network:** Perceptron, multilayer network, backpropagation, introduction to deep neural network	3
VII	**Computational learning:** Computational learning theory, PAC learning model, Sample complexity, VC Dimension, Ensemble learning	3
VIII	**Clustering:** k-means, adaptive hierarchical clustering, Gaussian mixture model	3
IX	**Machine Learning in VLSI Design:** A Taxonomy for Machine Learning in VLSI Design	3
X	**Machine Learning for Lithographic Process Models:** Masks, and Physical Design, Yield Enhancements, Machine Learning based Aging Analysis	6
XI	**Machine Learning Hardware:** Energy-Efficient Design of Advanced Machine Learning Hardware	3

References

1. Bishop, C. (2006). Pattern Recognition and Machine Learning. Berlin: Springer-Verlag.
2. Ethem Alpaydin, Introduction to Machine Learning, PHI
3. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning Data Mining,Inference,and Prediction
4. Elfadel, Ibrahim M., Duane S. Boning, and Xin Li, eds. Machine Learning in VLSI Computer-Aided Design. Springer, 2019.

VLS 5234: Physical Design	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Apply digital logic design from Register Transfer Level to Graphic Data Stream flow with Signoff check
2. Analyze static timing constraints synthesis, Unified Power Format, Logical Equivalence Check
3. Apply procedure involved in floorplan, placement and routing
4. Analyze clock tree synthesis, extraction and Physical Verification
5. Apply digital testing

Unit	Topics	No. of Hours
I	**VLSI Physical Design Flow:** Recap of CMOS logic gate design- RTL modelling and physical design of simple gates, Clocking strategies	4

II	**Design Constraints:** Technology File, Circuit Description, Static timing constraints synthesis, Unified Power Format, Logical Equivalence Check	6
III	**Floorplan:** Technology File, Circuit Description, Design Constraints, Design Planning, Power Planning, Macro Placement, Design of Floorplan. Placement: Global Placement, Detail Placement, Routing: Global Routing, Detail Routing MOOC: VLSI Physical Design: https://archive.nptel.ac.in/courses/106/105/106105161/	10
IV	**Clock tree synthesis:** Clock tree synthesis, Power Analysis, Resistance extraction, Capacitance extraction, Inductance and impedance (RLC) extraction, Back annotation and Physical Verification	6
V	**Digital Testing:** Introduction to Digital Testing - Fault modelling - Fault Simulation - Testing for Single stuck faults - Design for Testability (DFT) - Ad-Hoc DFT - Scan based designs - Built-In Self-Test (BIST)	10

References

1. https://archive.nptel.ac.in/courses/106/105/106105161/
2. Neil H. E. Weste, David Harris, Kamran Eshraghian, "Principles of CMOS VLSI Design: A systems perspective", Third Edition, Addison Wesley,2008
3. Majid Sarrafzadeh, C. K. Wong , "An introduction to VLSI physical design", McGraw Hill, 1996, ISBN 0070571945, 9780070571945, 334 pages
4. Khosrow Golshan, "Physical design essentials: an ASIC design implementation perspective", Springer, 2007, ISBN 0387366423, 9780387366425, 211 pages
5. Ban P. Wong, Anurag Mittal, Yu Cao, Greg Starr Contributor Ban P. Wong, Anurag Mittal, Yu Cao, "Nano-CMOS circuit and physical design", John Wiley and Sons, 2004, ISBN 0471466107, 9780471466109

ENP 5230: Entrepreneurship	**L**	**T**	**P**	**C**	**Total hours**
	3	**0**	**0**	**3**	**36**

Course Outcome:

1. Explain the importance of entrepreneurship and entrepreneurial development model, social responsibilities of business
2. Describe Entrepreneurial Traits and Factors affecting Entrepreneurship process
3. Discuss Business Start-up Process
4. Summarize a business and marketing plan for entrepreneurs.

Unit	Topics	No. of Hours
I	**Introduction to Entrepreneurship:**	6

	Meaning and Definition of Entrepreneurship-Employment vs Entrepreneurship, Theories of Entrepreneurship, approach to entrepreneurship, Entrepreneurs VS Manager	
II	**Entrepreneurial Traits:** Personality of an entrepreneur, Types of Entrepreneurs	5
III	**Process of Entrepreneurship:** Factors affecting Entrepreneurship process	6
IV	**Business Start-up Process:** Idea Generation, Scanning the Environment, Macro and Micro analysis	7
V	**Business Plan writing:** Points to be considered, Model Business plan	6
VI	**Case studies:** Indian and International Entrepreneurship	6

References

1. NVR Naidu and T. Krishna Rao, "Management and Entrepreneurship", IK International Publishing House Pvt. Ltd 2008.
2. Mohanthy Sangram Keshari, "Fundamentals of Entrepreneurship", PHI Publications, 2005

ESD 5232: IT Project Management	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome:

1. Illustrate the importance of project planning.
2. Discuss and demonstrate various tools applicable for different phases of the software project.
3. Illustrate the importance of Change management.
4. Illustrate the importance of team work and demonstrate the usefulness of tools in effective handling of the project.
5. Compare the problems in projects that don't follow the process and discuss new trends in software life cycle.

Unit	Topics	No. of Hours
I	**Software Project Planning:** Understand the Project Needs, Create the Project Plan, Diagnosing Project Planning Problems	3
II	**Estimation:** Elements of a Successful Estimate, Wideband Delphi Estimation, Other Estimation Techniques, Diagnosing Estimation Problems.	3

III	**Project Schedules:** Building the Project Schedule, Managing Multiple Projects, Use the Schedule to Manage Commitments, Diagnosing Scheduling Problems.	3
IV	**Reviews:** Inspections, Deskchecks, Walkthroughs, Code Reviews, Pair Programming, Use Inspections to Manage Commitments, Diagnosing Review Problems.	4
V	**Software Requirements:** Requirements Elicitation, Use Cases, Software Requirements Specification, Change Control, Introduce Software Requirements Carefully, Diagnosing Software Requirements Problems	4
VI	**Design and Programming:** Review the Design, Version Control with Subversion, Refactoring, Unit Testing, Use Automation, Be Careful with Existing Projects, Diagnosing Design and Programming Problems	4
VII	**Software Testing:** Test Plans and Test Cases, Test Execution, Defect Tracking and Triage, Test Environment and Performance Testing, Smoke Tests, Test Automation, Postmortem Reports, Using Software Testing Effectively, Diagnosing Software Testing Problems	4
VIII	**Understanding Change:** Why Change Fails, How to Make Change Succeed	3
IX	**Management and Leadership:** Take Responsibility, Do Everything Out in the Open, Manage the Organization, Manage Your Team	2
X	**Managing an Outsourced Project:** Prevent Major Sources of Project Failure, Management Issues in Outsourced Projects, Collaborate with the Vendor	3
XI	**Process Improvement:** Life Without a Software Process, Software Process Improvement, Moving Forward	3

References

1. "Applied Software Project Management", Jennifer Greene, Andrew Stellman (O'Reilly Publications), 2005.
2. "The Art of Project Management", Scott Berkun (O'Reilly Publications), 2005.

VLS 5251: Advanced VLSI Design Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Design and simulate various analog VLSI building blocks.
2. Design and simulate mixed signal circuits - ADCs and DACs.

Unit	Topics	No. of Hours
I	Design and simulate current sources, sinks and references	9
II	Design and simulate various amplifier configurations	15
III	Experiment with nonlinear and dynamic analog circuits	7
IV	Design and analyse various data converter architectures	5

References

1. "CMOS Circuit Design, Layout, and Simulation", Baker, Li, & Boyce, IEEE Press, 1998.
2. "Design of Analog CMOS Integrated Circuits", Razavi, McGraw-Hill, Inc., 2000.
3. "Analog Integrated Circuit Design", Johns & Martin, John Wiley & Sons, 1997.
4. "CMOS Analog Design, 2nd Ed.", Allen & Holberg, Oxford Univ. Press, 1987.
5. "Analysis and Design of Analog Integrated Circuit", Gray & Meyer, John Wiley & Sons, 1984.
6. "Analog VLSI", Mohammed Ismail, & Terri Fiez, McGraw-Hill, Inc.
7. "VLSI - Design Techniques for Analog and Digital Circuits", Geiger, Allen, & Strader, McGraw-Hill, Inc.,
8. Cadence user manual

VLS 5252: Low Power VLSI Design Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Experiment static and dynamic power components.
2. Implement static power reduction techniques.
3. Apply dynamic power reduction techniques.

Unit	Topics	No. of Hours
I	Power dissipation in CMOS: Dynamic and Static power components, dynamic power components	9
II	Static power reduction techniques for low power	15
III	Dynamic power reduction techniques for low power	12

References

1. "Low-Power CMOS VLSI Circuit Design",Kaushik Roy and Sharat C. Prasad, Wiley-Interscience.
2. "CMOS Low Power Digital Design", A. Chandrakasan & R. Brodersen, Kluwer Academic Pubs. 1995.
3. "Low Power Design Methodologies",J. Rabaey & M. Pedram, , Kluwer Academic Pubs. 1996.
4. "Low - Power Digital VLSI Design, Circuits and Systems", Bellaour & M.I. Elamstry ,Kluwer Academic Publishers, 1996.
5. S. Imam & M. Pedram, Kluwer Academic Publishers, 1998.
6. "Logic synthesis for Low - power VLSI Designs", B.G.K.Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998.

VLS 5253 Scripting for VLSI Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Experiment shell script programmatically using different features and debugging the code.
2. Operate SED & AWK commands to do more complex task in easy way.
3. Experiment PERL scripts that create and change scalar, array and hash variables.

Unit	Topics	No. of Hours
I	Linux Fundamentals	6
II	Version Control	3
III	Shell Scripting - power utilities	9
IV	Perl	6
V	Tcl/Tk	3
VI	Python	3

References

1. "Introduction to Linux - A Beginner's Guide", Machtelt Garrels
2. "Unix shell programming", Stephen G. Kochan, Patrick H. Wood
3. "Sed & awk ",Dale Dougherty, Arnold Robbins
4. "Programming Perl", Larry Wall, Tom Christiansen, Jon Orwant
5. https://nptel.ac.in/courses/117106113

VLS 5254: Universal Verification Methodology Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Apply object-oriented concepts
2. Analyze reusable UVM Verification Components
3. Evaluate testbench integration and stimulus generation and TLM

Unit	Topics	No. of Hours
I	UVM Methodology, Stimulus Modeling, Test and Testbench Classes	12
II	UVM component classes, Configuration, UVM Sequences, Connecting to a DUT	12
III	UVM Environment for Cross bar switch and SDRAM Controller or Memory model	12

References

1. Vanessa R. Cooper, "Getting started with UVM: A beginner's guide", Verilab publisher, 2013.
2. SystemVerilog 3.1a Language Reference Manual

VLS 5281: Advanced Logic Synthesis Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Apply behavioral level logic hardware description language into register transfer logic.
2. Apply constraints and synthesize the combinational and sequential digital circuits.
3. Analyze the area, power, and performance reports.

Unit	Topics	No. of Hours
I	Write register transfer logic level code for combinational and sequential digital systems	9
II	Perform logic synthesis of combinational and sequential circuit description in register transfer logic	18
III	Generate the synthesized netlist and analyse critical path delay, area, power, and performance of the digital system	9

References

1. IEEE Standard for Verilog® Hardware Description Language by IEEE Computer Society
2. Cadence manual for synthesis tool

VLS 5283: Machine Learning for VLSI Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Apply the software and tools for designing machine learning applications.
2. Apply concept learning and hypothesis space.
3. Analyze Artificial Neural Network, Clustering, Support Vector Machine, Deep Neural Network and Reinforcement Learning models, Support Vector Machine.

Unit	Topics	No. of Hours
I	Goals and applications of machine learning, Basic design issues and approaches to machine learning, Concept learning as search through a hypothesis space, General-to-specific ordering of hypotheses.	12
II	Probability theory and Bayes rule, Naive Bayes learning algorithm - Parameter smoothing, Logistic regression, Bayes nets and Markov nets for representing dependencies, Neurons and biological motivation, Activation functions and threshold units, Supervised and unsupervised learning, Perceptron Model: representational limitation and gradient descent training, Multilayer networks and back propagation, Overfitting.	12
III	Learning from unclassified data, Clustering. Hierarchical Aglomerative Clustering, Non-Hierarchical Clustering - k-means partitional clustering, Expectation maximization (EM) for soft clustering, Semi-supervised learning with EM using labeled and unlabled data, Maximum margin linear separators, Quadractic programming solution to finding maximum margin separators, Kernels for learning non-linear functions, Varying length pattern classification using SVM	12

References

1. Machine Learning, T. Mitchell, McGraw-Hill, 1997
2. Machine Learning, E. Alpaydin, MIT Press, 2010
3. Machine Learning for Big Data, Jason Bell, Wiley Big Data Series

VLS 5284: Physical Design Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Apply timing constraint and synthesize the digital circuit
2. Analyze Unified Power Format, Logical Equivalence Check and Design For Test
3. Analyze the steps involved in physical design and physical verification

Unit	Topics	No. of Hours
I	Perform logic synthesis of combinational and sequential circuit description in RTL: Ripple Carry, Carry Look-Ahead, Latch, Flip-flops, counters, FSMs	15
II	Perform physical design flow: Use floorplan, placement, clock tree synthesis and routing	15
III	Back annotation: Extract resistance, capacitance, inductance and simulate the design. Generate and analyse area, power, and performance reports	6

References

1. Cadence manual for synthesis and physical design tool

ENP 5280: Entrepreneurship Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Study of prominence of entrepreneurship.
2. Develop use cases for building a business.
3. Evaluation of factors influencing business venture.

Unit	Topics	No. of Hours
I	Study of use cases for need and prominence of entrepreneurship, associated decision making process.	6
II	Study of report by the National Knowledge Commission on the importance of entrepreneurship in economic development.	6
III	Develop use cases for identifying and evaluating opportunities, developing business plan, assessment of resources, project appraisal and feasibility plan.	9
IV	creating and starting venture includes legal requirements, marketing strategies, financial plans and human resources management	9
V	Design a Case studies of Indian and International Entrepreneurship.	6

References

1. Management and Entrepreneurship, NVR Naidu and T. Krishna Rao, IK International Publishing House Pvt.Ltd, 2008.
2. Fundamentals of Entrepreneurship, Mohanthy Sangram Keshari, PHI Learning Pvt. Ltd., 2005.

ESD 5282: IT Project Management Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome:

1. Identify the skills and techniques required for project life cycle.
2. Illustrate essential principles associated with project management and their application in business environment.
3. Outline commonly available project management tools.

Unit	Topics	No. of Hours
I	Software project management and its need, evaluation techniques, Project cost estimation techniques.	12
II	Activity scheduling techniques, cost monitoring, contract management and its necessity risk analysis.	12
III	Software quality enhancement techniques, people management in software environment and project team structure.	12

References

1. "Applied Software Project Management", Jennifer Greene, Andrew Stellman (O'Reilly Publications), 2005.
2. "The Art of Project Management", Scott Berkun (O'Reilly Publications), 2005.

MPT 5200 Mini project - II	L	T	P	C	Total hours
	0	0	0	4	48

Course Outcome:

1. Identify the real-world and socially relevant problems and perform feasibility analysis for finding solutions.
2. Organize work effectively as a member in a team, examine, experiment, and communicate technical information constructively.
3. Develop and implement solutions to the identified problems by applying research methodology and development life cycle with appropriate documentation by incorporating ethical standards.

Unit	Topics	No. of Hours
I	Problem identification, literature survey, formation of detailed specifications.	48
II	Design and implementation of the proposed system architecture.	
III	Demonstrate an ability to present and defend project work carried out to a panel of experts.	

References

1. Research articles and Online Resources.

PSD 5200: Professional Skill Development - II	L	T	P	C	Total hours
	0	0	0	1	12

Course Outcome:

1. Develop the skills needed for approaching technical and HR interviews.
2. Use mathematical, reasoning, and domain specific skills to solve objective questionnaires in time.
3. Demonstrate depth of knowledge in the chosen field of study.

Unit	Topics	No. of Hours
I	Peer interviews, mock interviews.	12
II	Logical reasoning, mathematical aptitude, domain specific problem solving skills.	
III	Conduction of domain specific knowledge test.	

References

1. R S Aggarwal. Quantitative Aptitude for Competitive Examinations. S Chand, 2017.
2. McDowell, Gayle Laakmann. Cracking the coding interview: 189 programming questions and solutions. CareerCup, LLC, 2015.
3. Domain specific tools and online resources.

VLS 6098: Project Work	L	T	P	C	Total hours
	0	0	0	25	300

Course Outcome:

1. Undertake innovative industry/research oriented projects and perform feasibility analysis for finding solutions.
2. Implement and test the proposed design using appropriate framework, programming language and tools.
3. Demonstrate an ability to present and defend project work carried out to a panel of experts.

Unit	Topics	No. of Hours
I	Problem identification, literature survey, formation of detailed requirement specification document.	300
II	Design and implementation of the proposed modules with specific test cases.	
III	Detailed report of the work carried out, present, and defend the project work carried out to a panel of experts.	

References

1. Research articles, domain specific tools and online resources.

Program Outcome and Course Outcome: Mapping

Sl. No.	Course Code	Course Name	Credits	PO1	PO2	PO3	PO4	PO5
1	VLS 5001	High Level Digital Design	3			*	*	
2	VLS 5101	Data Structures	3	*		*	*	
3	VLS 5102	Digital Systems and VLSI Design	3			*	*	*
4	VLS 5103	Verification	3			*	*	
5	VLS 5131	CAD for VLSI	3	*		*		*
	VLS 5132	System on chip Design	3			*	*	
	ESD 5001	Digital Signal Processing	3	*		*	*	
	MVT 5101	VLSI Fabrication Technology	3			*	*	
6	VLS 5051	High Level Digital Design Lab	1			*	*	*
7	VLS 5151	Data Structures Lab	1	*		*	*	
8	VLS 5152	Digital Systems and VLSI Design Lab	1			*	*	*
9	VLS 5153	Verification Lab	1			*	*	
10	VLS 5181	CAD for VLSI Lab	1	*		*		*
	VLS 5182	System on chip Design Lab	1				*	*
	ESD 5051	Digital Signal Processing Lab	1	*		*	*	
	MVT 5151	VLSI Fabrication Technology Lab	1			*	*	
11	MPT 5100	Mini Project - I	4	*	*	*	*	*
12	PSD 5100	Professional Skill Development - I	1	*	*			
13	VLS 5201	Advanced VLSI Design	3	*		*	*	*
14	VLS 5202	Low Power VLSI Design	3	*		*	*	*
15	VLS 5203	Scripting for VLSI	3	*		*	*	
16	VLS 5204	Universal Verification Methodology	3			*	*	

17	VLS 5231	Advanced Logic Synthesis	3			*	*	
	VLS 5233	Machine learning for VLSI Design	3			*	*	
	VLS 5234	Physical Design	3			*	*	
	ENP 5230	Entrepreneurship	3			*	*	
	ESD 5232	IT Project Management	3	*		*		*
18	VLS 5251	Advanced VLSI Design Lab	1	*		*	*	*
19	VLS 5252	Low Power VLSI Design Lab	1	*		*	*	*
20	VLS 5253	Scripting for VLSI Lab	1	*		*	*	
21	VLS 5254	Universal Verification Methodology Lab	1				*	*
22	VLS 5281	Advanced Logic Synthesis Lab	1			*	*	
	VLS 5283	Machine Learning for VLSI Design Lab	1			*	*	
	VLS 5284	Physical Design Lab	1				*	*
	ENP 5280	Entrepreneurship Lab	1			*	*	
	ESD 5282	IT Project Management Lab	1	*		*		*
23	MPT 5200	Mini Project - II	4	*	*	*	*	*
24	PSD 5200	Professional Skill Development - II	1			*	*	*
25	VLS 6098	Project Work	25	*	*	*	*	*

Manipal Academy of Higher Education, Manipal

Master of Engineering - ME Programs offered at

Manipal School of Information Sciences (MSIS), Manipal

Rules and Regulations

(Applicable to the students admitted to the Master of Engineering - M.E. (Specialization) programs from July 2024)

1. TITLE OF THE PROGRAMS:

Post Graduate Degree Programs: As per the AICTE Approval

- Master of Engineering - **M.E. (Artificial Intelligence and Machine Learning)**
- Master of Engineering - **M.E. (Big Data Analytics)**
- Master of Engineering - **M.E. (Cloud Computing)**
- Master of Engineering - **M.E. (Cyber Security)**
- Master of Engineering - **M.E. (Embedded Systems)**
- Master of Engineering - **M.E. (Microelectronics and VLSI Technology)**
- Master of Engineering - **M.E. (VLSI Design)**

Degree to be awarded: Master of Engineering - M.E. (Specialization)

2. ELIGIBILTY CRITERIA:

- Eligibility criteria for the students seeking admission to the Master of Engineering - ME Programs are:

Program Name	Eligibility
M.E. (Artificial Intelligence and Machine Learning) M.E. (Big Data Analytics) M.E. (Cloud Computing) M.E. (Cyber Security)	• Candidate with BE / BTech in *Electrical or Circuit Stream* or *Computer Science Stream* or *equivalent* with a minimum of 50% pass from a recognized university. • Candidate with BE/ BTech in *other stream* with a minimum of 50% pass from a recognized university. A programming skills test will be conducted at the Institute to select the candidate in this category. Admission to this category is based on the availability of seats. An optional bridge course will be conducted.
M.E. (Embedded Systems)	Candidate with BE / BTech in *Electrical or Circuit Stream* or *Computer Science Stream* or *equivalent* with a minimum of 50% pass from a recognized university.
M.E. (VLSI Design) M.E. (Microelectronics and VLSI Technology)	Candidate with BE / BTech in *Electrical or Circuit Stream* or *Computer Science Stream* or *equivalent* with a minimum of 50% pass from a recognized university.

3. DURATION OF THE PROGRAMS:

3.1 Normal Duration - 2 Years

3.2 Maximum permissible duration of the program is 4 years. Students who fail to complete the program within this stipulated maximum duration will not be eligible for the award of the degree.

3.3 Semester I and II of the programs are made up of about 16 weeks of classes and related academic activities followed by about 2 to 3 weeks of end-semester examinations.

3.4 The program will have first year (semesters I & II) of study at MSIS and second year (semesters III & IV) of the program is exclusively for the Project Work in an industry or in a research organization or in an educational institution.

4. EDUCATIONAL PROCESS

4.1 CREDIT BASED SYSTEM

4.1.1 The educational process at MSIS uses a credit-based system, wherein the course content is expressed in a number of credits.

4.1.2 The content of individual courses - theory as well as practical - is expressed in terms of a certain number of credits. The number of credits assigned to a course depends on the number of contact hours per week. Normally, in the case of theory courses, the number of credits is equal to the number of contact hours (lectures & tutorials) per week, while in the case of practical courses, one credit is assigned for every three contact hours per week.

4.1.3 A student is deemed to have successfully completed a particular semester's program of study when he / she earns all the credits of that semester, i.e., he / she has no "F" grade in any course of that semester.

4.1.4 When a student earns the specified number of credits in all the courses of the program, he / she is deemed to have completed the requirements for graduation. This also means a student should have an "E" grade or better in every course of every semester to be eligible to receive the degree.

4.1.3 The second year (semesters III & IV) of the program is exclusively for Project Work. The minimum duration of the Project Work is 10 months from the date of commencement.

4.1.4 As part of the academic requirements, students must do Project Work of 10 to 12 months duration in one or more industries or institutes in any country. A mid-term project presentation must be given between 5-7 months from the start date of the Project Work.

4.1.5 A student becomes eligible for the final presentation after completing a minimum of 3 months of work from the date of mid-presentation subject to fulfilling the total minimum Project Work duration of 10 months.

4.1.6 If any extension of Project Work beyond 12 months is required, students can get approval from the institute.

4.1.7 A student cannot join any organization as a full-time employee before the completion of Project Work.

4.1.9 A student will be eligible for the final presentation only after completing the following: (i) the midterm presentation and the required minimum duration as specified in Section 4.1.4. (ii) A feedback email and project review approval from the external guide (iii) Internship Completion Certificate issued by the respective industry where the students carryout their internship; and (iii) Project review approval from the internal guide at MSIS.

4.2 OUTLINE OF EVALUATION

4.2.1 The system makes use of a continuous evaluation process.

4.2.2 Students' performance in each ***Theory*** course is evaluated out of a maximum of 100 marks, of which 50 are for in-semester assessment and 50 are for end-semester examinations.

4.2.3 Students' performance in each ***Lab*** course is evaluated out of a maximum of 100 marks, of which 50 are for in-semester assessment and 50 are for end-semester examinations.

4.2.4 Students' performance in ***Professional Skill Development and a Mini Project*** will be evaluated internally for a maximum of 100 marks.

4.2.5 In-semester assessment will be based on continuous evaluation, which includes assignments, case presentations, class tests, quizzes, etc.

4.2.6 Students' performance in assignments, case presentations, etc. will be properly documented and announced before finalizing the IA marks.

4.2.7 A faculty committee headed by the Director will investigate all grievances of students regarding their performance in internal tests, practical tests, mid-semester and end-semester examinations.

4.2.8 The overall performance of a student in each course is expressed in terms of a Letter Grade. This uses the Relative Grading System.

4.2.9 For Theory courses, the evaluation of the answer scripts for the end semester exam is carried out by the faculty who taught the course.

4.2.10 Students viewing of the evaluated answer papers will be enabled for TWO days. Students can view the answer scripts using their login credentials.

4.2.11 Students who have doubts in the evaluated answer scripts can approach the respective course coordinator for clarification.

4.2.12 In the end semester exam, if a student gets an **F** or **I** grade in the course(s), s/he will be eligible to appear for the make-up exam.

4.2.13 A make-up exam for Theory and Lab courses will be conducted within a month for the students who get an F, or I grade in the End Semester Examination.

4.2.14 If a student gets an F or I grade in the make-up examination, s/he will be eligible to appear for the course exam only after ONE YEAR.

4.2.15 If a student does not register for the make-up exam, s/he will be eligible to appear for the course exam only after ONE YEAR.

4.2.16 Marks scored from in-semester evaluation and end-semester evaluation (for a maximum of 100 marks as in 4.2.2 to 4.2.4) will be considered to award the grade for all the Theory and Lab courses.

4.2.17 The SLCM system facilitates the processing and dissemination of examination results, typically within a week following the conclusion of the examination period.

4.2.18 The GPA and CGPA for the students are calculated as given in Section 4.6.2.4.

4.2.19 The midterm presentation of the Project Work should be completed between 5-7 months from the date of joining for the Project Work and is evaluated for 100 marks by the internal guide at MSIS. The final project viva voce examination is evaluated by two examiners for 300 marks. The maximum mark for the Project Work is 400. The Project Work uses a fixed grading system, as in 4.8.5.

4.3 PROGRAM ADVISORY COMMITTEE (PAC) MEETING

4.3.1 The PAC will meet at least once a semester to discuss the broad assessment procedure for the current semester, the results of the previous mid-semester / end-semester examination, the performance of the students in the program of study, improving the effectiveness of the teaching-learning processes, and a plan of action for the next semester.

4.3.2 The program coordinator may send the minutes of the meeting to the Director and other attendees after each PAC meeting.

4.4 ATTENDANCE REQUIREMENTS

4.4.1 Under the relative grading system, a student must maintain an attendance record of at least 75% in every course.

4.4.2 Without the minimum attendance, the student becomes ineligible for the mid-semester examination, the end-semester examination, and subsequent grading during that semester.

4.4.3 The student must attend the classes for the detained course(s) in the next available semester in which the course is taught and get 75% attendance to become eligible to write the mid-semester and end-semester examinations.

4.4.4. However, there is no minimum attendance requirement during the Project Work.

4.5 PROMOTION TO HIGHER SEMESTER-ACADEMIC PERFORMANCE REQUIREMENTS

4.5.1 Promotion of a student from one semester to the next higher semester is subject to his / her fulfilling the minimum attendance requirement as in 4.4.1 and is not the only criterion to be met for the fulfillment of the academic performance requirements.

4.5.2 As far as the academic requirements are concerned, the system is a full carry-over system.

4.5.3 A student can commence the Project Work at the beginning of the second year, but he / she must earn all the credits of the first year before he / she is permitted to

submit the Project Work for the final project viva voce examination. Further, he / she must complete the program within the maximum period stipulated for the award of the degree.

4.6 EVALUATION PROCEDURE

4.6.1. SEMESTER EVALUATION

4.6.1.1 All Theory and Lab courses taken by students during the semester are evaluated using an internal system of continuous assessment and the end-semester evaluation.

4.6.1.2 The student may be evaluated based on class participation, assignment work, lab work, internal tests, mid-semester and end-semester examinations, which contribute to the final grade awarded for the course.

4.6.1.4 Students will be informed at the commencement of each semester about the evaluation methods being used for each course and the weights given to the different components of each course by the concerned course coordinator (in the course plan).

4.6.1.5 In-semester (internal) assessment in each course is evaluated for 50 marks, which includes performances in class participation, assignment work, lab work, internal tests, mid-semester examination, etc.

4.6.1.6 The end-semester examination for each Theory course is evaluated for a maximum of 100 marks, and the same will be scaled down to 50.

4.6.1.7 End-semester marks for a maximum of 50 and internal assessment marks for a maximum of 50 are added for a maximum of 100 marks to decide upon the grade in each course.

4.6.1.8 End-semester examinations will be conducted for each Theory and Lab course at the end of every semester.

4.6.1.9 If a student gets an F/I grade in the course(s) in the end-semester exam, s/he will be eligible to appear for the make-up exam.

4.6.1.10 Make-up exam for Theory and Lab courses will be conducted within a month for the students who get an F, or I grade in the end semester examination.

4.6.1.11 If a student gets an F or I grade in the make-up exam, s/he will be eligible to appear for the course(s) exam only after **ONE YEAR.**

4.6.1.12 Even if a student has not registered for this make-up exam, s/he will be eligible to appear for the course(s) exam only after **ONE YEAR.**

4.6.1.13 If a student gets an F or I grade in the end semester examination and clears the course in the make-up examination, s/he will get a maximum of a C grade.

4.6.2. Relative Grading:

4.6.2.1 Marks obtained as mentioned in 4.2.2 to 4.2.4 are considered in the relative grading system to award a letter grade for each of the courses.

4.6.2.2 The grade cutoff generated in SLCM for each course will be used for result processing.

4.6.2.3 The results will be declared through the SLCM system, and the students can view the results using their login credentials.

4.6.2.4 The GPA for the students will be calculated for the current semester, and the CGPA will be calculated based on the accumulated grade points from the first semester onwards of the program.

4.6.2.5 A student will fail in either Theory or Lab, or both, if he/she fails to score a minimum of 40% in the end semester examination and 40% aggregate as in Section 4.2 (adding internal and end semester marks together) in each course.

4.6.3 Letter Grading System:

The final evaluation of the student in a course is carried out on a 10-point grading system, which is as follows:

PERFORMANCE GRADE

Grade Points	10	9	8	7	6	5	0
Grade	A+	A	B	C	D	E	F (Fail)

4.6.3.1 A student who earns a minimum of 5 grade points ("E" grade) in a course is declared to have successfully completed that course.

4.6.3.2 A student should have appeared for the end-semester examination of the prescribed course of study to be eligible for the award of the grade in that course.

4.6.3.3 If a student is eligible but fails to appear in the end-semester examination, he/she will be awarded an "I" grade (incomplete) on the grade sheet. For all practical purposes, an "I" grade is treated as an "F" grade.

4.6.3.4 In the event that a student receives an "F" or "I" grade for a course during the end semester examination but subsequently passes the course during a makeup examination without re-registration, the highest possible grade that may be awarded is a "C".

4.6.4 Grade Point Average, (GPA) and Cumulative Grade Point Average (CGPA):

Each course grade is converted into a specific number of points associated with the grade. These points are weighted in accordance with the number of credits assigned to a course. The grade point average for each semester will be calculated only for those students who have passed all the courses of that semester. The weighted average of GPAs of all semesters that the student has completed at any point of time is the cumulative grade point average (CGPA) at that point of time.

CGPA up to any semester will be calculated only for those students who have passed all the courses up to that semester.

Calculation of GPA and CGPA:
Example:

course	Credits	Letter Grade	Grade Value	Credit Value	Grade Points
Course 1	3	C	7	3 x 7	21
Course 2	3	B	8	3 x 8	24
Course 3	3	A	9	3 x 9	27
Course 4	2	B	8	2 x 8	16
Total	11			Total	88

$$\text{In this case GPA} = \frac{\text{Total grade points}}{\text{Credits}} = \frac{88}{11} = 8.0$$

Suppose the GPA in two successive semesters is 7.0 and 8.0 with 26 and 24 respective credits in those semesters, then the

$$\text{CGPA} = \frac{7.0 * 26 + 8.0 * 24}{26 + 24} = \frac{374}{50} = 7.48$$

Generally,

$$\text{GPA} = \frac{\sum_{i=1}^{n} CiGi}{\sum_{i=1}^{n} Ci} \quad \& \quad \text{CGPA} = \frac{\sum_{j=1}^{N}(GPAj * \sum Ci)j}{\sum_{j=1}^{N}(\sum Ci)j}$$

Here,
n = Number of courses
Ci = Number of Credits of i^{th} course
N = Number of semesters
Gi = Grade of the i^{th} course

After the results are declared, grade report cards will be issued to each student, which will contain the list of courses of that semester, the grades obtained by the student in those courses, GPA and CGPA.

4.6.5 RE-REGISTRATION

4.6.5.1 Students who are detained in a particular semester due to shortage of attendance is not eligible to attend the examinations, can re-register in one or more courses of that semester in which they are detained (in the semester in which those courses are offered) by paying, the prescribed fees.

4.6.5.2 If a student is interested in improving GPA in a semester, he / she may re-register for all the courses of that semester by paying the prescribed fees.

Student must attend the classes, write the tests, assignments, and end-semester examinations of all the courses of that semester for which he / she has re-registered for improvement of GPA. When a student re-registers for the improvement in a semester, the attendance, IA marks and GPA obtained in that semester in the previous attempt becomes **null and void.** Students re-registering for improvement of GPA of a semester must surrender his/her original grade report card along with the re-registration application. Actual grade will be awarded.

4.6.5.3 A student can re-register for the improvement on the GPA of a semester within 15 days from the date of announcement of the result.

4.6.5.4 Students can re-register in one or more courses offered in current semester (both Theory and Labs) within 15 days from the date of announcement of the result for internal assessment improvement after paying the prescribed fees if they have got "F"/ "I" grades earlier. They can attend the classes in the next available semester in which the course is taught, must submit assignments, appear for internal tests, mid-semester and end-semester examinations. Actual grade will be awarded. However, re-registration will be allowed only with prior permission of the Director.

4.6.5.5 A student cannot re-register for the improvement of the grades in individual courses.

4.7. REQUIREMENTS FOR GRADUATION

A student is deemed to have completed the requirements for graduation if he / she has:

4.7.1 Fulfilled all minimum requirements in prescribed courses of study and earned the number of credits specified in the program of study.

4.7.2 Satisfied with all rules of evaluation.

4.7.3 Satisfied the requirements specified by the Institution, if any.

4.7.4 Cleared all dues.

4.7.5 No case of indiscipline pending against him / her.

4.8 DECLARATION OF THE RESULT

4.8.1 After the completion of the end-semester evaluation, marks secured for a maximum of 100 marks (50 for internal evaluation and 50 for end semester evaluation) of all the students will be compiled course-wise.

4.8.2 The cut off marks and the grades in each course based on the credit system guidelines will be decided through SLCM.

4.8.3 The results will be declared through SLCM.

4.8.4 A student will fail in either Theory or Lab or both if he / she fails to score a minimum of 40% in the end semester and 40% aggregate as in Section 4.2 (internal & end semester together) in each course.

4.8.5 The Project Work in the second year (third & fourth semesters) use the following fixed

grading system.

Grade	Range
A+	90 % - 100 %
A	80 % - 89.99 %
B	70 % - 79.99 %
C	60 % - 69.99 %
D	50 % - 59.99 %
E	40 % - 49.99 %
F	< 40 %

4.9 Award of Degree

4.9.1 Students who successfully complete the program by earning the required number of credits within the stipulated maximum duration of the program are awarded the degree with CGPA.

4.9.2 As per MAHE guidelines, credits earned from the partner university / institute are considered for the award of the degree but not for the calculation of GPA / CGPA. Thus, MAHE will issue a certificate for the credits earned from the partner university, but not a Grade Report for those credits.

4.9.3 Number of credits to be earned for the award of Master of Engineering - M.E. Degree program is 75.

4.9.4 Graduates who have earned **all credits from MAHE** will be eligible for consideration for the Gold Medal being awarded at the time of Convocation.

(These rules and regulations are subject to change / amendment from time to time, as and when need arises)

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