MANIPAL
ACADEMY *of* HIGHER EDUCATION
(Institution of Eminence Deemed to be University)

Master of Engineering - ME (VLSI Design)

Syllabus

July 2022 Onwards

MANIPAL SCHOOL OF INFORMATION SCIENCES
MANIPAL ACADEMY OF HIGHER EDUCATION
MANIPAL – 576104.KARNATAKA. INDIA.

Program Educational Objectives / Outcomes (PEOs)

PEO 1: Successfully engage in challenging careers with professional approach in the areas of analog & digital VLSI design and related domains of engineering.

PEO 2: Demonstrate competence in identifying and analyzing technical problems, suggest feasible and innovative solutions using their core competence in VLSI design and thereby support the technological growth of the nation.

PEO 3: Impart quality technical education, engage in research and contribute to knowledge creation and sharing.

PEO 4: Possess analytical, communicative and leadership skills, and demonstrate the ability to work in multidisciplinary and multi-cultural environments.

PEO 5: Be Self-motivated and remain continuously employable by engaging in lifelong learning.

Program Objectives / Outcomes (POs)

PO1 Scholarship of Knowledge: Acquire in-depth knowledge of VLSI domain, with an ability to discriminate, evaluate, analyze, synthesize the existing and new knowledge, and integration of the same for enhancement of knowledge.

PO2 Critical Thinking: Analyze complex VLSI Eco System critically; apply independent judgement for synthesizing information to make intellectual and/or creative advances for conducting research in a wider theoretical, practical and policy context.

PO3 Problem Solving: Think laterally and originally, conceptualize and solve VLSI Design problems, evaluate a wide range of potential solutions for those problems and arrive at feasible, optimal solutions after considering public health and safety, cultural, societal and environmental factors in the core areas of expertise.

PO4 Research Skill: Extract information pertinent to unfamiliar problems through literature survey and experiments, apply appropriate research methodologies, techniques and tools, design, conduct experiments, analyze and interpret data, demonstrate higher order skill and view things in a broader perspective, contribute individually/in group(s) to the development of scientific/technological knowledge in one or more domains of engineering.

PO5 Usage of modern tools: Create, select, learn and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modelling, to complex engineering activities with an understanding of the limitations.

PO6 Collaborative and Multidisciplinary work: Possess knowledge and understanding of group dynamics, recognize opportunities and contribute positively to collaborative-multidisciplinary scientific research, demonstrate a capacity for self-management and teamwork, decision-making based on open-mindedness, objectivity and rational analysis in order to achieve common goals and further the learning of themselves as well as others.

PO7 Project Management and Finance: Demonstrate knowledge and understanding of engineering and management principles and apply the same to one's own work, as a member and leader in a team, manage projects efficiently in respective disciplines and multidisciplinary environments after consideration of economic and financial factors

PO8 Communication: Communicate with the engineering community, and with society at large, regarding complex engineering activities confidently and effectively, such as, being able to comprehend and write effective reports and design documentation by adhering to appropriate standards, make effective presentations, and give and receive clear instructions.

PO9 Life-long Learning: Recognize the need for and have the preparation and ability to engage in life-long learning independently, with a high level of enthusiasm and commitment to improve knowledge and competence continuously.

PO10 Ethical Practices and Social Responsibility: Acquire professional and intellectual integrity, professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

PO11 Independent and Reflective Learning: Observe and examine critically the outcomes of one's actions and make corrective measures subsequently and learn from mistakes without depending on external feedback.

Program Structure

ME (VLSI Design) – I Semester									
Course Code	Course Name	No. of Hrs./week				Duration of Exam in Hrs	Maximum Marks		
		Lecture	Tutorial	Practical	Credit		Internal 50	External 50	Total 100
VLS 5001	High Level Digital Design	3	-	-	3	3	50	50	100
VLS 5101	Data Structures	3	-	-	3	3	50	50	100
VLS 5102	Digital Systems & VLSI Design	3	-	-	3	3	50	50	100
VLS 5103	Verification	3	-	-	3	3	50	50	100
	Elective – I	3	-	-	3	3	50	50	100
VLS 5051	High Level Digital Design Lab	-	-	3	1	3	50	50	100
VLS 5151	Data Structures Lab	-	-	3	1	3	50	50	100
VLS 5152	Digital Systems & VLSI Design Lab	-	-	3	1	3	50	50	100
VLS 5153	Verification Lab	-	-	3	1	3	50	50	100
	Elective - I Lab	-	-	3	1	3	50	50	100
MPT 5100	Mini Project - I	-	-	-	4	-	100	-	100
PSD 5100	Professional Skill Development - I	-	-	-	1	-	100	-	100
Total		**15**	**-**	**15**	**25**				

ME (VLSI Design) – II Semester									
Course Code	Course Name	No. of Hrs. / week				Duration of Exam in Hrs	Maximum Marks		
		Lecture	Tutorial	Practical	Credit		Internal 50	External 50	Total 100
VLS 5201	Advanced VLSI Design	3	-	-	3	3	50	50	100
VLS 5202	Low Power VLSI Design	3	-	-	3	3	50	50	100
VLS 5203	Scripting for VLSI	3	-	-	3	3	50	50	100
VLS 5204	Universal Verification Methodology	3	-	-	3	3	50	50	100
	Elective – II	3	-	-	3	3	50	50	100
VLS 5251	Advanced VLSI Design Lab	-	-	3	1	3	50	50	100
VLS 5252	Low Power VLSI Design Lab	-	-	3	1	3	50	50	100
VLS 5253	Scripting for VLSI Lab	-	-	3	1	3	50	50	100
VLS 5254	Universal Verification Methodology Lab	-	-	3	1	3	50	50	100
	Elective - II Lab	-	-	3	1	3	50	50	100
MPT 5200	Mini Project - II	-	-	-	4	-	100	-	100
PSD 5200	Professional Skill Development - II	-	-	-	1	-	100	-	100
TOTAL		**15**	**-**	**15**	**25**				

ME (VLSI Design) -III & IV Semesters									
VLS 6098	Project Work	-	-	-	25				
Total Number of Credits to Award Degree							75		

List of Electives (Theory)

Elective - I		Elective - II	
Course Code	**Course Name**	**Course Code**	**Course Name**
VLS 5131	CAD for VLSI	VLS 5231	Advanced Logic Synthesis
VLS 5132	System on Chip Design	VLS 5232	Formal Methods
ESD 5001	Digital Signal Processing	VLS 5233	Machine Learning for VLSI Design
		VLS 5234	Physical Design
		VLS 5235	Wireless Communications and Antenna Design
		ENP 5230	Entrepreneurship
		ESD 5232	IT Project Management
		ESD 5236	System Software

List of Electives (Lab)

Elective - I		Elective - II	
Course Code	**Course Name**	**Course Code**	**Course Name**
VLS 5181	CAD for VLSI Lab	VLS 5281	Advanced Logic Synthesis Lab
VLS 5182	System on Chip Design Lab	VLS 5282	Formal Methods Lab
ESD 5051	Digital Signal Processing Lab	VLS 5283	Machine Learning for VLSI Design Lab
		VLS 5284	Physical Design Lab
		VLS 5285	Wireless Communications and Antenna Design Lab
		ENP 5280	Entrepreneurship Lab
		ESD 5282	IT Project Management Lab
		ESD 5286	System Software Lab

SEMESTER I

VLS 5001: High Level Digital Design	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome

1. Describe digital design and apply digital logic to solve real life problems
2. Apply sequential logic circuits and timing analysis
3. Describe FPGA, FIFO, and AMBA bus designs

Unit	Topics	No. of Hours
I	Introduction: Digital System; VLSI design Flow	2
II	Combinational Design: Number System: Binary; 1's Complement; 2's Complement. Single Precision, Double precision	1
III	Arithmetic Circuits: Ripple Carry, Carry Look-Ahead, Carry Skip, Carry Increment, Tree Adder: Brent Kung, Sklansky, Kogge Stone Adder	2
IV	Datapath Functional Units: Comparator; Funnel Shifter, Multi Input Adder; Multiplier; Divider.	2
V	Optimization: logic optimization techniques, Branch method, Petrick Methods	3
VI	Sequential Design: Latch; Flip-flops; scan Flip-flop; Registers Set; Design of counters	2
VII	FSM: Mealy Machine; Moore Machine; Mixed Machine, FSM optimization	4
VIII	Timing Analysis: Foundry Library; Liberty format; Gates: Propagation Delays; Flops: Propagation Delay; Setup time; hold Time; contamination delay; Recovery time; Removal time; Clock frequency; Jitter; Skew(source & network latency); Timing Paths; Multi-input path; Clock Budget; Multi-Clock; Multi-Cycle Path; False Path; Retiming	6
IX	Introduction to FPGA: PLD; FPGA design flow	2

X	FPGA: Introduction to FPGA Boards	4
XI	Digital Design Application: FIFO Design-1; FIFO Design-2 [SNUG Papers]	4
XII	AMBA Bus Specification: AHB; APB	4

References

1. "An Engineering Approach to Digital Design" , Flectcher
2. "Rapid Prototyping of Digital Systems - SOPC Edition", James O Hamblen, Tyson S Hall, Michael D Furman
3. "Simulation and Synthesis Techniques for Asynchronous FIFO Design", Clifford E. Cummings [SNUG Paper]
4. "Simulation and Synthesis Techniques for Asynchronous FIFO Design with Asynchronous Pointer Comparisons", Clifford E Cummings, Peter Alfke [SNUG Paper]
5. ARM Specification2.0

VLS 5101: Data Structures	**L**	**T**	**P**	**C**	**Total hours**
	3	**0**	**0**	**3**	**36**

Course Outcome

1. Design programs for implementation of linked lists, stack and queues.
2. Design programs for implementation of binary search tree, sorting and searching, dictionary and Hash Table
3. Design programs for graphs and shortest path techniques.

Unit	**Topics**	**No. of Hours**
I	**Algorithm specification and analysis techniques:** Analysis of recursive programs. Solving recurrence equations. General solution for a large class of recurrences.	3
II	**Elementary data structures** : Implementation of Array, lists, stacks, queues, Trees	17
III	**Sorting & Searching: B**ubble, selection, insertion, Quick sort, heap sort, merge sort. Linear search and binary search.	6
IV	**Hash Tables and Graph:** Hashing and Dictionaries.Representation of graphs. Depth First Searching. Breadth First Searching,Minimum cost spanning tree. Single source shortest paths and all-pairs shortest path	10

References

1. "Data Structures& Algorithms" Aho, Hopcroft and Ulmann
2. "Data structures and algorithm analysis in C", Mark Allen Weiss
3. "Computer Algorithms", Ellis Horowitz, Sartaj Sahni, Sanguthevar Rajasekaran
4. Introduction to Algorithms - Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest. MIT Press.

VLS 5102: Digital Systems & VLSI Design	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome

1. Understand static and dynamic behavior of MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) and the secondary effects of the MOS transistor model.
2. Be able to design and test static CMOS combinational and sequential logic at the transistor level, including mask layout.
3. To provide experience designing integrated circuits using Computer Aided Design (CAD) Tools
4. Describe the general processing technologies of CMOS integrated circuits.

Unit	Topics	No. of Hours
I	**MOS transistor theory:** Ideal I-V Characteristics, C-V Characteristics, CMOS inverter – DC Characteristics, Noise Margin, Static load MOS inverters, NELS, NELT, HMOS, Pass transistor, Transmission gate, tristate inverter, MOSFET Models, Non-ideal I-V effects.	10
II	**CMOS circuit and layout design:** Combinational and Sequential Circuit Design, Basic physical design of simple gates, CMOS logic structures (Dynamic CMOS Logic, C2MOS Logic, CMOS and NP Domino	4
III	**Circuit characterization:** Resistance estimation, Capacitance estimation, delay time calculation, principles of modelling the gate, Switching characteristics, CMOS gate transistor sizing, Power dissipation, Scaling principles	7

IV	**CMOS Subsystem Design:** Data path operations - Adder, Comparator, Counter, Semiconductor memory elements - SRAM, DRAM	5
V	**CMOS Technologies:** Wafer Formation, Photolithography, Well and Channel Formation, Silicon Dioxide (SiO2), Oxidation, Isolation Gate Oxide, Gate and Source/Drain Formations, Contacts and Metallization, Passivation, SOI.	5
VI	**Layout Design Rules:** Design Rule Background, Micron and Lambda Design Rules	4
VII	**Manufacturing Issues:** Antenna Rules, Layer Density Rules, Resolution Enhancement Rules.	1

References

1. "CMOS digital integrated circuits analysis and design", Kang Sung Mo and Leblebici Yusuf, McGraw Hill, 1999.
2. "Principles of CMOS VLSI Design: A systems perspective", 2nd Edition, Neil H. E. Weste, Kamran Eshraghian, Addison Wesley, 1999.
3. "CMOS VLSI Design: A circuits & systems perspective", 3rd Edition, Neil H. E. Weste, David Harris, Addison Wesley, 2007.
4. "Microchip Fabrication", by Peter Van Zant, 5th Edition, McGraw-Hill, International Edition.

VLS 5103: Verification	**L**	**T**	**P**	**C**	**Total hours**
	3	**0**	**0**	**3**	**36**

Course Outcome

1. Describe types of verification, verification plan including assertions for the digital VLSI circuits.
2. Apply verification environments and test cases for various designs and create reusable verification IP.
3. Explain the coverage metrics for verification process, assertions, extensible verification components, software test environments, and post silicon validation.

Unit	**Topics**	**No. of Hours**
I	**Introduction:** Verification Challenges, Productivity, Design for Verification, Methodology	2

II	**Types of Verifications & Approaches:** Formal Verification, Property Based Verification, Functional Verification, Rule Checking-Linting, Black Box Verification, White Box Verification, Grey Box Verification	3
III	**Verification Planning:** Planning Process, Response Checking	2
IV	**Assertions:** Specifying Assertions, Assertions on Internal DUT Signals, Assertions on External Interfaces, Assertion Coding Guidelines, Reusable Assertion-Based, Qualification of Assertions	5
V	**Test bench Infrastructure:** Testbench Architecture, Simulation Control, Data and Transactions, Transactors, Transaction-Level Interfaces, Timing Interface, Callback Methods, Ad-Hoc Testbenches, Legacy Bus-Functional Model	8
VI	**Stimulus and Response:** Generating Stimulus, Controlling Random Generation, Self-Checking Structures	4
VII	**Coverage-Driven Verification:** Coverage Metrics, Coverage Models, Functional Coverage Implementation, Feedback Mechanisms.	3
VIII	**Assertions for Formal Tools:** Model Checking and Assertions, Assertions on Data	2
IX	**System-Level Verification:** Extensible Verification Components, XVC Manager, System-Level Verification Environments, Verifying Transaction-Level Models, Hardware-Assisted Verification.	3
X	**Processor Integration Verification:** Software Test Environments, Structure of Software Tests, Test Actions	3
XI	**Post-Silicon SoC Validation:** Introduction, Validation Activities, Planning for Post-Silicon Readiness, Post-Silicon Debug Infrastructure, Generation of Tests, Post-Silicon Debug	1

References

1. Janick Bergeron, Verification methodology manual for SystemVerilog, Springer.
2. Janick Bergeron, Writing Testbenches using System Verilog, Springer.
3. William K. Lam, Hardware Design Verification - Simulation and Formal Method Based Approaches.
4. Pallab Dasgupta, A Roadmap for Formal Property Verification, Springer

ELECTIVES - SEMESTER I

VLS 5131: CAD for VLSI	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome

1. Explain various VLSI design flows, design methods and technologies.
2. Describe various VLSI design steps and relevant design automation tools, Explain types of synthesis, Illustrate design representations and graph based problem formulations.
3. Illustrate and apply CAD algorithms used in VLSI design automation.

Unit	Topics	No. of Hours
I	**Introduction to VLSI Design Methodologies:** The VLSI deign problem, Design domains, Design Actions, Design methods and technologies	6
II	**Review of VLSI Design Automation Tools :** Quick tour of design automation tools for various methods and levels of VLSI design, Physical Design, Verification, Design Management	8
III	**High Level Synthesis :** Introduction to Synthesis, Design representations and transformations	3
IV	**High Level Synthesis Algorithms**: Partitioning, Scheduling, Allocation algorithms	10
V	**Floor Planning and Placement :** Floor planning concepts, Shape Functions and Floor plan sizing, Placement, Types of placement problems and algorithms	3
VI	**Routing:** Local routing, Types of local routing problems, Area and Channel routing problems and algorithms, Global routing	3
VII	**Layout Compaction:** Design rules, symbolic layout, Algorithms for layout compaction.	3

References

1. "Graph theory" , Narsingh Deo (Prentice-Hall of India private ltd)
2. "Graph theory" , Gibbons
3. "Algorithms for VLSI Design Automation" ,Sabih H. Gerez (John Wiley and Sons)

4. "High Level Synthesis -Introduction to chip and System Design" , Daniel Gajski, Nikil Dutt, Allen Wu, Steve Lin (Kluwer Academic Publishers)
5. "Logic synthesis and verification algorithms" , Gary D. Hachtel, Fabio Somenzi (Kluwer Academic Publishers)
6. "Computer aided logical design with emphasis on VLSI " , Frederick J Hill, Gerald R. Peterson (john Wiley & sons)

VLS 5132: System on Chip Design	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome

1. Describe system architecture, identify hardware software co-design, give examples of co-design space, explain specification & modelling, pre-partition, partition, analyse post-partition analysis, and describe hardware and software implementation.
2. Review the processors and its micro-architecture and basic elements in instruction handling, recognize robust processors.
3. Describe on and off-die memories, explain memories in system on chip, compare memory systems, cache memory, model memories, interconnects in system on chip, explain network on chip.

Unit	Topics	No. of Hours
I	**Introduction to System Approach:** System Architecture overview, Components of the System, Introducing Hardware/Software Codesign, The Driving Factors of Hardware/Software Design, The Hardware-Software Codesign space.	3
II	**Electronic System Level Flow:** Specification and Modeling, Pre-Partitioning Analysis, Partitioning, Post-Partitioning Analysis and Debug, Post-Partitioning Verification, Hardware Implementation, Software Implementation.	4
III	**Design Principles in SOC Architecture:** Heterogeneous & Distributed Data Processing, Heterogeneous & Distributed Data Communications, Heterogeneous & Distributed Data Storage, Hierarchical Control.	3
IV	**Processors:**	6

	Introduction to Processors, Processor Selection for SOC, Basic Concepts in Processor Architecture, RISC Pipeline, Basic Concepts in Processor Microarchitecture, Basic Elements in Instruction Handling, Buffers, Branches, Robust Processors	
V	**Memory Design:** Introduction, Overview of SOC Internal and External Memories, Scratchpads and Cache Memory, Cache Organization, Cache Data, Write Policies, Strategies for Line Replacement at Miss Time, Other Types of Caches, Split I- and D-Caches and the Effect of Code Density, Multilevel Caches, Virtual-to-Real Translation, SOC (On-Die) Memory Systems, Board-Based (Off-Die) Memory systems, Simple DRAM and the Memory Array, Models of Simple Processor-Memory Interaction.	6
VI	**Hardware Interconnects:** Introduction, Overview of Interconnect Architectures, Bus Architecture, SOC Standard Buses, Analytic Bus Models, Beyond the Bus (NOC with Switch Interconnects), Some NOC Switch Examples, Layered Architecture and Network Interface Unit, Evaluating Interconnect Networks.	4
VII	**Hardware/Software Interfaces:** Introduction, Synchronization Schemes, Memory-Mapped Interfaces, Coprocessor Interfaces, Custom-Instruction Interfaces.	3
VIII	**Application Studies:** 3-D Graphics Processor / Software Defined Radio with 802.16, Universal Serial Bus	7

References

1. Michael J. Flynn , Wayne Luk, “Computer System Design System-On-Chip”, John Wiley & Sons, Inc., Publication, 2011.
2. Brain Bailey, Grant Martin, Andrew Piziali, “ESL Design and Verification: A Prescription for Electronic System-Level Methodology”, Morgan Kaufmann Publication, 2007.
3. Patrick R. Schaumont, “A Practical Introduction to Hardware/Software Codesign”, Springer, 2010.
4. Don Anderson, USB System Architecture (USB 2.0), Mindshare, Inc., 2001.

ESD 5001: Digital Signal Processing	**L**	**T**	**P**	**C**	**Total hours**
	3	**0**	**0**	**3**	**36**

Course Outcome

1. Analyze Fast Fourier Transform (FFT) algorithms on computational complexity.
2. Design IIR and FIR filters using various sampling techniques.
3. Interpret Multirate Signal Processing and Adaptive Filters.
4. Infer architecture, memory management and pipelining concepts of General and TMS320C67XX Digital Signal Processor.

Unit	Topics	No. of Hours
I	**Review: (Self Study):** Introduction Classification of signals and systems, brief discussions on z-transform, inverse z-transform & Fourier transform, DFT, linear convolution using circular convolution & DFT	
II	**FFT Algorithms:** Radix-2 DIT-FFT Algorithm, DIF-FFT Algorithm. Assignments (Problems).	3
III	**Filter Structures:** IIR Filter Structure – Direct Form I & II, CSOS, PSOS & Transpose structures - FIR Filter Structures – Direct Form, Cascade form, Linear Phase Filter structures. Assignments (Problems).	5
IV	**Design of FIR filters:** Using Frequency Sampling & Windows - Assignments (Problems).	5
V	**Design of IIR Filters:** Butterworth & Chebychev filters design using impulse invariance & bilinear transformation techniques, Design of IIR filter using pole placement technique. Assignments (Problems).	7
VI	**Multirate Signal Processing:** Decimation, Interpolation, Sampling rate conversion by a rational factor, structures, Polyphase filter structures, Time variant Filter structure, Application of Multirate signal processing to Phase Shifter, Subband coding of Speech signal, Digital Filter Bank Implementation, QMF Filter bank	10

VII	**Adaptive Filters:** Class of Optimal Filters – Predictive Configuration, Filter Configuration, Concept of adaptive noise cancellation, Noise Canceller Configuration. LMS adaptive Algorithm, Application of LMS algorithm to the optimal filter configurations. Adaptive noise canceller as a high-pass filter	3
VIII	**DSP Processor:** Introduction to PDSPs – Multiplier and Multiplier Accumulator (MAC), Modified Bus structures and memory access schemes, Multiple access memory, Multiported Memory, VLIW architecture, Pipelining, Special Addressing modes, On-chip Peripherals. TMS320C6711 DSP processor: Architecture, Instruction set and assembly language programming	3

References

1. Sanjith K Mitra, "Digital Signal Processing", McGraw Hill Education, 4th Edition, July 2013.
2. Oppenheim and Schafer, "Digital Signal Processing", Pearson, First Edition, 1975.
3. Roman Kuc, "Digital Signal Processing", McGraw-Hill Education, 1988.
4. Proakis and Manolakis, "Digital Signal Processing", Prentice – Hall, Inc., Third Edition, 1996.
5. Rabinder and Gold, "Theory and Application of Digital Signal Processing", Prentice Hall India Learning Private Limited, 1988.
6. Hwei P Hsu, Schaum's Outline of "Signals and Systems", 3rd Edition, 2013.
7. Symon Haykins, "Signals and Systems", Wiley, Second Edition, 2002.

VLS 5051: High Level Digital Design Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Design and Simulate combinational circuits using Verilog and SystemVerilog.
2. Analyze sequential logic circuits and timing analysis by simulating and synthesis procedure.
3. Experiment Datapath Functional Units by design and simulation procedure.

Unit	Topics	No. of Hours

I	Design and Simulation of combinational circuits: Number System: Binary; 1's Complement; 2's Complement, Ripple Carry, Carry Look-Ahead, Carry Skip, Carry Increment, Tree Adder: Brent Kung, Sklansky, Kogge Stone Adder	12
II	Design and Simulation of sequential circuits: Latch; Flip-flops; scan Flip-flop Registers Set; Design of counters, Mealy Machine; Moore Machine; Mixed Machine	12
III	Design and Simulation of Datapath Functional Units and advanced Digital Systems: Comparator; Funnel Shifter, Multi Input Adder, Multiplier; Divider, FIFO Design	12

References

1. Sutherland, S., et al. "SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling, vol. 2." (2006).
2. SystemVerilog 3.1a Language Reference Manual

VLS 5151: Data Structures Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Analyze recursive programs, solve a general class of recurrence relations.
2. Design programs for implementation of linked lists, stack, queues, binary search tree, sorting and searching.
3. Design programs for sorting and searching.
4. Design programs for dictionary, hash tables, graphs and shortest path techniques.

Unit	Topics	No. of Hours
I	**Algorithm specification and analysis techniques:** Analysis of recursive programs. Solving recurrence equations. General solution for a large class of recurrences.	3
II	**Elementary data structures :** Implementation of Array, lists, stacks, queues, Trees	18

III	**Sorting & Searching:** Bubble, selection, insertion sort, Quick sort, heap sort, merge sort. Linear search and binary search.	6
IV	**Hash Tables and Graph:** Implement Hashing and Dictionaries, graphs. Depth First Searching. Breadth First Search, Minimum cost spanning tree. Single source shortest paths.	9

References

1. Introduction to Algorithms - Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest. MIT Press.
2. Data Structures and Algorithms - Aho, Hopcroft and Ulmann. Pearson Publishers.

VLS 5152: Digital Systems & VLSI Design Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Simulate MOSFET, pass transistor, and Transmission gate characteristics.
2. Design and simulate simple combinational and sequential circuits using Cadence Virtuoso.
3. Draw layout of simple digital circuits, carryout DRC and LVS.

Unit	Topics	No. of Hours
I	**MOS transistor theory, CMOS circuit and layout design:** I-V Characteristics of NMOS, PMOS, CMOS inverter – DC characteristics, Transfer Characteristics, Noise Margin, Pass transistor, Transmission gate, tristate inverter, Design and simulation of simple Combinational and Sequential Circuits, CMOS logic structures (Dynamic CMOS Logic, C2MOS Logic, CMOS and NP Domino Logic)	15
II	**Circuit characterization and CMOS Subsystem Design:** Resistance estimation, Capacitance estimation, delay time calculation, principles of modelling the gate, Switching characteristics, CMOS gate transistor sizing, Power dissipation. Data path operations - Adder, Comparator, Counter, Semiconductor memory elements - SRAM, DRAM	15
III	**Study of CMOS Technologies, DRC and Manufacturing Issues:** Basic physical design of simple gates, combinational and sequential circuits DRC, LVS, Study of Antenna Rules, Layer Density Rules, Resolution Enhancement Rules	6

References
1. "CMOS digital integrated circuits analysis and design", Kang Sung Mo and Leblebici Yusuf, McGraw Hill, 1999. 2. "Principles of CMOS VLSI Design: A systems perspective", 2nd Edition, Neil H. E. Weste, Kamran Eshraghian, Addison Wesley, 1999. 3. "CMOS VLSI Design: A circuits & systems perspective", 3rd Edition, Neil H. E. Weste, David Harris, Addison Wesley, 2007. 4. Cadence User manual.

VLS 5153: Verification Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Analyze simulation with direct and random test vectors for combinational circuits using Verilog and SystemVerilog.
2. Describe sequential logic circuit simulation with SystemVerilog constructs.
3. Construct the verification environment for Datapath Functional Units and simulate.

Unit	Topics	No. of Hours
I	Simulate and verify combinational circuits: Number System: Binary; 1's Complement; 2's Complement. Single Precision, Double precision, Ripple Carry, Carry Look-Ahead, Carry Skip, Carry Increment, Tree Adder: Brent Kung, Sklansky, Kogge Stone Adder,	12
II	Simulate and verify sequential circuits: Latch; Flip-flops; scan Flip-flop; Registers Set; Design of counters, Mealy Machine; Moore Machine; Mixed Machine	12
III	Construct verification environment for the verification of Datapath Functional Units: Comparator; Funnel Shifter, Multi Input Adder; Multiplier; Divider, FIFO Design, AMBA Bus Protocols	12

References

1. Spear, Chris. SystemVerilog for verification: a guide to learning the testbench language features. Springer Science & Business Media, 2008.
2. SystemVerilog 3.1a Language Reference Manual

VLS 5181: CAD for VLSI Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Experiment data structures for design representations using graphs.
2. Develop programs to implement high level synthesis algorithms.
3. Develop programs to implement physical design algorithms.

Unit	Topics	No. of Hours
I	Introduction to Synthesis, Design representations and transformations	9
II	High level synthesis algorithms	18
III	Physical design algorithms	9

References

1. “Graph theory” , Narsingh Deo (Prentice-Hall of India private ltd)
2. “Algorithms for VLSI Design Automation” , Sabih H. Gerez (John Wiley and Sons)
3. “High Level Synthesis -Introduction to chip and System Design” , Daniel Gajski, Nikil Dutt, Allen Wu, Steve Lin (Kluwer Academic Publishers)

VLS 5182: System on Chip Design Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Design of different SOC Architecture.
2. Design of simple Processors and Memory.
3. Practice 3-D Graphics Processor / Software Defined Radio with 802.16, Universal Serial Bus.

Unit	Topics	No. of Hours
I	Partitioning, Post-Partitioning Analysis and Debug, Post-Partitioning Verification, Hardware Implementation, Software Implementation.	7
II	Design of various SOC Architecture - Heterogeneous & Distributed Data Processing, Heterogeneous & Distributed Data Communications, Heterogeneous & Distributed Data Storage, Hierarchical Control.	10
III	Design an simulation of simple Processors	6
IV	Design and simulation of Memory - Simple DRAM and the Memory Array, Models of Simple Processor-Memory Interaction	6
V	Study of 3-D Graphics Processor / Software Defined Radio with 802.16, Universal Serial Bus	7

References

1. Michael J. Flynn , Wayne Luk, "Computer System Design System-On-Chip", John Wiley & Sons, Inc., Publication, 2011.
2. Brain Bailey, Grant Martin, Andrew Piziali, "ESL Design and Verification: A Prescription for Electronic System-Level Methodology", Morgan Kaufmann Publication, 2007.
3. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Codesign", Springer, 2010.
4. Don Anderson, USB System Architecture (USB 2.0), Mindshare, Inc., 2001.

ESD 5051: Digital Signal Processing Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Practice the usage of MATLAB software tool.
2. Design and analysis of various filter structures using MATLAB – FIR filters, IIR filters, Adaptive filters.
3. Experiment the usage of DSP processors - TMS320C6711 DSP processes.

Unit	Topics	No. of Hours
I	To get acquainted with the use of MATLAB software tool	6
II	Design and analysis of various filter structures using MATLAB – FIR filters, IIR filters, Adaptive filters	21
III	Study and use of DSP processors - TMS320C6711 DSP processes.	9

References

1. Sanjith K Mitra, "Digital Signal Processing", McGraw Hill Education, 4th Edition, July 2013.
2. Oppenheim and Schafer, "Digital Signal Processing", Pearson, First Edition, 1975.
3. Roman Kuc, "Digital Signal Processing", McGraw-Hill Education, 1988.
4. Proakis and Manolakis, "Digital Signal Processing", Prentice – Hall, Inc., Third Edition, 1996.
5. Rabinder and Gold, "Theory and Application of Digital Signal Processing", Prentice Hall India Learning Private Limited, 1988.
6. Hwei P Hsu, Schaum's Outline of "Signals and Systems", 3rd Edition, 2013.
7. Symon Haykins, "Signals and Systems", Wiley, Second Edition, 2002.

MPT 5100: Mini Project - I	L	T	P	C	Total hours
	0	0	0	4	48

Course Outcome

1. Identify the real-world and social relevant problems and perform feasibility analysis for finding solution.
2. Develop solutions to the identified problems by applying research methodology and development life cycle with appropriate documentation by incorporating ethical standards.
3. Work effectively as a member in a team and communicate technical information effectively.

Unit	Topics	No. of Hours
I	Problem identification, literature survey, formation of detailed specifications.	48
II	Design and implementation of the proposed system architecture.	
III	Demonstrate an ability to present and defend project work carried out to a panel of experts.	

References

1. Research articles and Online Resources.

PSD 5100: Professional Skill Development - I	L	T	P	C	Total hours
	0	0	0	1	12

Course Outcome

1. Identify and synthesize important themes in the field of engineering which transform socio-economic ecosystem.
2. Develop competence to communicate effectively in oral and written forms.
3. Effective management of time, involve in reflective learning and adhere to the professional code of conduct.

Unit	Topics	No. of Hours

I	Report writing involves identifying the topic of interest from current issues in the domain of engineering and technology or inter disciplinary domains, then framing the order in the report, writing abstract, deciding on the content itself, conclusion and future scope of the topic and properly citing the references from bibliography.	12
II	Presenting in classroom to audience where content spoken, the conceptual knowledge and presentation skills (like audibility, eye contact, memory) of speaker is assessed.	
References		
1. Research articles and Online Resources.		

SEMESTER II

VLS 5201: Advanced VLSI Design	**L**	**T**	**P**	**C**	**Total hours**
	3	**0**	**0**	**3**	**36**

Course Outcome

1. To learn modeling, analysis, and design of analog circuits using CMOS technologies.
2. Introduce the principles of analog circuits and apply the techniques for the design of CMOS analog integrated circuits.
3. Apply the methods learned in the class to design and implement practical projects

Unit	**Topics**	**No. of Hours**
I	**CMOS passive elements:** Resistor: Fabrication–Different layers used, Layout techniques and practical considerations, Temperature and voltage dependence resistors, Active resistors – advantages, Capacitor: Fabrication – "poly-substrate", "poly-poly", "metal-poly" – comparison, Layout techniques, Temperature and voltage dependence, Active Capacitors.	3

II	**Analog MOSFET Models:** Low frequency MOSFET Model: Small-signal model of the MOSFET in saturation, Derivation for g_m and r_0 High frequency MOSFET Model: Variation of transconductance with frequency	1
III	**Current Sources and Sinks:** Current Source, current Sink and Current Mirror – Differences, Applications ,Current Mirror-Basic current mirror, The cascode current mirror – advantages, derivation ,for o/p resistance r0,Layout of current Sources/Sinks/Mirrors, Matching in MOSFET mirrors, Other Current Sources /Sinks/Mirrors- Wilson current mirror, Regulated cascode current mirror	3
IV	**References:** Voltage Dividers, Sensitivity and Fractional temperature coefficients-Resistor-MOSFET divider, MOSFET-only voltage divider, Current Source Self-Biasing-Threshold voltage referenced self-biasing, Diode referenced self-biasing, Thermal voltage referenced self-biasing, Bandgap voltage references, Bandgap referenced biasing, Beta Multiplier Referenced Self-Biasing-A voltage reference, Operation in the Sub-threshold region	4
V	**CMOS Single Stage Amplifiers:** Amplification – need for amplification, basic concepts, Important performance parameters – "Analog Design Octagon" ,Common Source (CS) Amplifier-Derivation for Av and comparison of CS Amplifier with: Passive resistor load, MOSFET/Diode-Connected/ /Active load, Current source load - Common Drain Amplifier (or Source Follower)-Derivation for Av and comparison of CD Amplifier with: Passive resistor load, MOSFET/Diode-Connected/ /Active load, Current source load - Common Gate Amplifier-Derivation for Av and comparison of CG Amplifier with: Passive resistor load, MOSFET/Diode-Connected/ /Active load, Current source load - The Push-Pull Amplifier, Noise and Distortion in Amplifiers-A class AB Amplifier - Modeling Amplifier Noise	6
VI	**Differential Amplifiers:** The Source Coupled Pair- Current Source Load, Common-Mode Rejection Ratio, Noise, Matching Considerations. The Source Cross-Coupled Pair-Current Source Load Cascode Loads, Wide-Swing Differential Amplifiers, Current Differential Amplifier, Constant Transconductance Diff-Amp.	4

VII	**Frequency Response of Amplifiers:** Introduction, Frequency response of single stage amplifiers, Frequency response of Differential pair.	3
VIII	**Noise:** Statistical characteristics of noise, types of noise, representation of noise in circuits, noise in single-stage amplifiers, noise in differential pairs, noise bandwidth.	3
IX	**Operational Amplifiers:** Basic CMOS Op-Amp Design-Characterizing the op-Amp, Compensating the Op-amp Without Buffer, The Cascode Input Op-amp, Operational Transconductance Amplifiers.	2
X	**Nonlinear Analog Circuits:** Design of Basic CMOS Comparator, Characterizing the Comparator Adaptive Biasing, Analog Multipliers- The Multiplying Quad, Level Shifting, Multiplier Design Using Squaring Circuits.	2
XI	**Dynamic Analog Circuits:** The MOSFET Switch - Switched-Capacitor Integrator Circuits	2
XII	**Data Converter Fundamentals and Architectures**: Sample-and-Hold (S\H) Characteristics, DAC and ADC Specifications, Architectures – Cyclic DAC, Pipeline DAC, Pipeline ADC, Integrating ADCs, SAR ADC	3

References

1. "CMOS Circuit Design, Layout, and Simulation", Baker, Li, & Boyce, IEEE Press, 1998.
2. "Design of Analog CMOS Integrated Circuits", Razavi, McGraw-Hill, Inc., 2000.
3. "Analog Integrated Circuit Design ", Johns & Martin, , John Wiley & Sons, 1997.
4. "CMOS Analog Design, 2nd Ed." ,Allen & Holberg, Oxford Univ. Press, 1987.
5. "Analysis and Design of Analog Integrated Circuits ",Gray & Meyer, John Wiley & Sons, 1984.
6. "Analog VLSI" ,Mohammed Ismail, & Terri Fiez, , McGraw-Hill, Inc.
7. "VLSI - Design Techniques for Analog and Digital Circuits",Geiger, Allen, & Strader McGraw-Hill, Inc.,
8. Recent papers from IEEE Journal of Solid state Circuits and other technical magazines

VLS 5202: Low Power VLSI Design	**L**	**T**	**P**	**C**	**Total hours**
	3	**0**	**0**	**3**	**36**

Course Outcome

1. Describe various components of power in CMOS VLSI Design.
2. Comprehend various leakage power reduction techniques, technology and scaling related aspects of low power VLSI design.
3. Explain dynamic power reduction techniques and system level issues.

Unit	Topics	No. of Hours
I	**Introduction to Low Power Design**	2
II	**Overview of power dissipation in CMOS**: Dynamic and Static power components, Leakage current components, Factors affecting leakage power, Examples	5
III	**Circuit techniques for leakage power reduction:** Stacking – natural and artificial, Multiple V_{th} techniques - Multiple Channel Doping's, Multiple Oxide CMOS (MOXCMOS) Circuits, Multiple Channel Lengths, Multiple Body Biases, Multi-threshold-voltage CMOS (MTCMOS), Dual Threshold CMOS, Variable Threshold CMOS (VTMOS), Dynamic Threshold CMOS (DTMOS), Dynamic V_{th} techniques – V_{th} hopping scheme, Dynamic voltage scaling (DVTS) scheme.	8
IV	**Technology scaling for dynamic power reduction:** Scaling techniques – constant voltage, constant field and lateral scaling. **Voltage scaling approaches:** Reliability-Driven Voltage Scaling, Technology-Driven Voltage Scaling, Energy x Delay Minimum Based Voltage Scaling, Voltage Scaling through Optimal Transistor Sizing, Voltage Scaling using Threshold Reduction, Architecture-Driven Voltage Scaling.	8
V	**Glitch power**: Generated and propagated glitches, Glitch power analysis, Reduction techniques, Gate triggering approach.	3
VI	**Clock gating**: Principle, Combinational and sequential clock gating, Clock gating efficiency.	2
VII	Adiabatic techniques for low power	2

IX	Logic optimization for low power, Power modelling, Power analysis	2
X	System level issues in multi-voltage designs, Level shifters	2
XI	Low power design of building blocks	2

References

1. "Low-Power CMOS VLSI Circuit Design", Kaushik Roy and Sharat C. Prasad, Wiley-Interscience.
2. "CMOS Low Power Digital Design", A. Chandrakasan & R. Brodersen, Kluwer Academic Pubs. 1995.
3. "Low Power Design Methodologies", J. Rabaey & M. Pedram, , Kluwer Academic Pubs. 1996.
4. "Low – Power Digital VLSI Design, Circuits and Systems", Bellaour & M.I. Elamstry ,Kluwer Academic Publishers, 1996.
5. S. Imam & M. Pedram, Kluwer Academic Publishers, 1998.
6. "Logic synthesis for Low – power VLSI Designs", B.G.K.Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998.
7. "Power Aware Design Methodologies", Pedram, Massoud, Rabaey, Jan M., Kluwer Academic Publishers.
8. "Low-power Digital Systems Based on Adiabatic- Switching Principles", W.C. Athas, L. Swensson, J.G. Koller and E. Chou, , IEEE Transactions on VLSI Systems, vol. 2, pp. 398-407, December 1994.
9. "A survey of power estimation techniques in VLSI circuits", F. Najm, IEEE Transactions on VLSI Systems, vol. 2, pp. 446-455, December 1994.

VLS 5203: Scripting for VLSI	**L**	**T**	**P**	**C**	**Total hours**
	3	**0**	**0**	**3**	**36**

Course Outcome

1. Discover shell script programmatically using different features and debugging the code.
2. Apply SED & AWK commands to do more complex task in easy way.
3. Apply PERL scripts that create and change scalar, array and hash variables.

Unit	**Topics**	**No. of Hours**

I	OS, h/w, kernel, File system, Process, Networking, Version control	5
II	Variables,Arithmetic,echo, Quotes, Redirection, pipe, filters, Wild cards , exit status Command line arguments, constructs, Constructs	5
III	Cut , paste , tr, uniq	1
IV	Sed, Grep	4
V	Awk and Make	5
VI	Introduction, command line, Pattern matching, Subroutines, Formats, References, Packages, Modules, Threads , overloading	16

References

1. "Introduction to Linux – A Beginner's Guide", Machtelt Garrels
2. "Unix shell programming", Stephen G. Kochan, Patrick H. Wood
3. "Sed & awk", Dale Dougherty, Arnold Robbins
4. "Programming Perl", Larry Wall, Tom Christiansen, Jon Orwant

VLS 5204: Universal Verification Methodology	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome

1. Model a scenario for Verification of a DUT in UVM.
2. Analyze the usefulness of a driver, monitor, checker, test cases in UVM verification environment.
3. Explain component configuration and factory, Register Abstraction Layer and TLM communications
4. Design test bench to verify the functionality of a design.
5. Design a VIP for an IP as a project.

Unit	Topics	No. of Hours
I	UVM overview: Verification Planning and Coverage-Driven Verification, Multi-Language and Methodologies. UVM Testbench and environments, Interface UVCs, System and Module UVCs, the System Verilog UVM class library	2

II	Object Oriented Programming: Introduction, What is an object in OOP, Distributed development environment, Classes, Objects, Programs, Using generalization and inheritance, polymorphism in OOP, Downcast, Class libraries, Static methods and attributes, parameterized classes, packages and namespaces	3
III	UVM library basics: Using UVM library, Library Base Classes, the uvm_object class, the uvm_component class, UVM configuration mechanism, TLM in UVM, UVM factory, UVM message facilities, callbacks.	2
IV	Interface UVCs: Stimulus modeling and generation, creating the driver, creating the sequencer, connecting the driver and sequencer	5
V	Automating UVC Creation: Creating the collector and monitor, modeling topology with UVM, creating the Agent, creating the UVM verification component, creating UVM sequences, configuring the sequencer's default sequence, coordinating end-of-test, implementing protocol-specific coverage and checks, handling reset, packaging interface UVCs	3
VI	Component Configuration and Factory: Establish and Query Component Parent-Child Relationships, Set Up Component Virtual SystemVerilog Interfaces with uvm_config_db, Constructing Components and Transactions with UVM Factory, Implement Tests to Configure Components, Implement Tests to Override Components with Modified Behavior	3
VII	UVM Callback: Create User Callback Hooks in Component Methods, Implement Error Injection with User Defined Callbacks, Implement Component Functional Coverage with User Defined Callbacks, Review Default Callbacks in UVM Base Class.	2
VIII	Simple Testbench integration: Testbenches and Tests, creating a simple testbench, testbench configuration, creating a test, creating meaningful tests, virtual sequencers and sequences, checking for DUT correctness, implementing a coverage model.	4
IX	Stimulus generation topics: Fine control sequence generation, executing multiple sequences concurrently, using p_sequencer, using pre_body() and post_body() methods, controlling the arbitration of items, interrupt sequences, protocol layering.	2
X	Register Abstraction Layer: Registers, Specification, Adapter, Integrating, Integration, Register Model Overview, Model Structure, Quirky Registers, Model	4

	Coverage, Back Door Access, Generation, Stimulus Abstraction, Memory Stimulus, Sequence Examples, Built in Sequences, Scoreboarding, Functional Coverage.	
XI	System UVCs and Testbench Integration: Introduction, module and system UVC architecture, sub-components of module and system UVCs, module UVC configuration, the testbench, sequences, coverage, stand-In mode, scalability concerns in system verification, module UVC Directory structure.	3
XII	TLM Communications: TLM Push, Pull and Fifo Modes, TLM Analysis Ports, TLM Pass-Through Ports, TLM 2.0 Blocking and Non-Blocking Transport Sockets	3

References

1. Sharon Rosenberg, Kathleen Meade, "A Practical Guide to Adopting the Universal Verification Methodology (UVM)", Lulu publishers, 2010.
2. Vanessa R. Cooper, "Getting started with UVM: A beginner's guide", Verilab publisher, 2013.
3. UVM Cookbook, Verification Academy, 2013.
4. UVM User's guide, Accellera, 2011.

ELECTIVES - SEMESTER II

VLS 5231: Advanced Logic Synthesis	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome

1. Describe logic synthesis process.
2. Explain procedure involved in logic synthesis of combinational and sequential circuits.
3. Classify multilevel logic synthesis and technology mapping.

Unit	Topics	No. of Hours
I	Introduction to logic synthesis	1

II	**Two-level logic synthesis:** Introduction, Boolean algebra concepts, Minimization using k-map, Minimization using Tabular method, Consensus theorem, Iterative Consensus theorem , Recursive computation, Unate covering problem a) Reduction technique b) MIS algorithm c) Branch and bound algorithm	14
III	**Sequential logic synthesis:** Introduction, Basics of FSM concept, Minimization of completely specified FSM, Equivalent partition algorithm, Minimization of Incompletely specified FSM, Compatible table, Maximum compatibles, Prime compatibles, Binate covering problem, FSM traversal algorithms, Depth first search, Breadth first search, Shortest path, State encoding and optimization	13
IV	**Multilevel logic synthesis:** Introduction, Algebraic and Boolean Division, Kernels and Cokernels Algebraic and Boolean resubtitution methods	5
V	**Technology mapping:** Graph covering and Technology mapping, Tree covering by Dynamic programming, Decomposition, Delay optimization and Graph covering	3

References

1. "Logic Synthesis and Verification Algorithms",Gary D. Hachtel and Fabio Somenzi (Kluwer Academic Publishers)
2. "Logic Minimization Algorithms For VLSI Synthesis" ,Robert K. Brayton ,Gary D. Hachtel, Curtis T. McMullen and Alberto L. Sangiovanni-Vincentelli (Kluwer Academic Publishers)

VLS 5232: Formal Methods	**L**	**T**	**P**	**C**	**Total hours**
	3	**0**	**0**	**3**	**36**

Course Outcome

1. Understand the relevance of formal methods in hardware and software design
2. Describe the theoretical foundations of formal methods
3. Explain the contemporary technologies for formal verification

Unit	Topics	No. of Hours
I	**The relevance of formal methods in hardware and software design:** Comparison to standard methods: simulation, and testing, the difficulty in adopting formal methods in industry, the state of the art in formal verification of systems, Nondeterministic systems, Reactive systems, and real-time systems, Different approaches to formal methods, Specification and verification of reactive systems, Model checking real-time systems, Program verification.	3
II	**Theoretical foundations of formal methods:** Formal specification, First-order logic for sequential systems, Temporal logic for reactive systems, Transition systems, Timed automaton for real-time specification, Specification of system properties, safety properties, progress properties: fairness and starvation, partial correctness and total correctness, Formal verification, Explicit state model checking, Symbolic model checking, Sequential program verification	15
III	**Contemporary technologies for formal verification:** NuSMV 2 for hardware verification, Simulation and Model checking, Spin for concurrent reactive system verification, Simulation and Model checking, UPPAAL for real-time systems	18

References

1. Logic in Computer Science: Modeling and Reasoning about Systems, Second edition, Michael Huth and Mark Ryan, Cambridge University Press.
2. Principles of Model Checking, Christel Baier and Joost-Pieter Katoen, MIT Press.
3. Model Checking, Edmund M. Clarke Jr., Orna Grumberg, and Doron A. Peled, MIT Press.
4. The SPIN Model Checker - Primer and Reference Manual. Gerard Holzmann, Addison-Wesley
5. NuSMV: http://nusmv.fbk.eu/
6. UPPAAL: http://www.it.uu.se/research/group/darts/uppaal/index.shtml
7. SPIN: http://spinroot.com/

VLS 5233: Machine Learning for VLSI Design	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome

1. Identify the goals, applications, types and design issues of machine learning techniques.
2. Analyse different machine learning algorithms.
3. Describe machine learning in VLSI computer-aided design.

Unit	Topics	No. of Hours
I	**Introduction**: Aims and applications of machine learning, learning systems, various aspects of developing a learning system	3
II	**Linear and Logistic Regression:** Linear regression, Decision trees, overfitting	3
III	**Instance based learning:** Instance based learning, Feature reduction, Collaborative filtering-based recommendation	3
IV	**Bayesian learning:** Probability and Bayes learning	3
V	**Logistic Regression:** Logistic Regression, Support Vector Machine, Kernel function and Kernel SVM	3
VI	**Neural network:** Perceptron, multilayer network, backpropagation, introduction to deep neural network	3
VII	**Computational learning:** Computational learning theory, PAC learning model, Sample complexity, VC Dimension, Ensemble learning	3
VIII	**Clustering**: k-means, adaptive hierarchical clustering, Gaussian mixture model	3
IX	**Machine Learning in VLSI Design:** A Taxonomy for Machine Learning in VLSI Design	3
X	**Machine Learning for Lithographic Process Models**: Masks, and Physical Design, Yield Enhancements, Machine Learning based Aging Analysis	6
XI	**Machine Learning Hardware:** Energy-Efficient Design of Advanced Machine Learning Hardware	3

References

1. Bishop, C. (2006). Pattern Recognition and Machine Learning. Berlin: Springer-Verlag.
2. Ethem Alpaydin, Introduction to Machine Learning, PHI
3. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning Data Mining,Inference,and Prediction

4. Elfadel, Ibrahim M., Duane S. Boning, and Xin Li, eds. Machine Learning in VLSI Computer-Aided Design. Springer, 2019.

VLS 5234: Physical Design	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome

1. Describe CMOS logic gate design, identify physical design of simple gates, give examples logic structures.
2. Explain procedure involved in floorplan step, placement, clock tree synthesis, routing, and extraction of layout.
3. Classify digital testing, give examples of fault modelling and fault simulation, test single stuck at faults, describe design for testability, ad-hoc DFT, scan based designs, built-in self-test.

Unit	Topics	No. of Hours
I	**CMOS circuit and layout design:** CMOS logic gate design- Basic physical design of simple gates - CMOS logic structures - Clocking strategies	3
II	**Floorplan:** Technology File, Circuit Description, Design Constraints , Design Planning, Power Planning, Macro Placement, Design of Floorplan	4
III	**Placement:** Global Placement, Detail Placement	3
IV	**Clock tree synthesis:** Clock tree synthesis, Power Analysis	6
V	**Routing:** Global Routing, Detail Routing	6
VI	**RC extraction:** Resistance extraction, Capacitance extraction, Inductance and impedance (RLC) extraction	4
VII	**Back annotation:** Back annotation procedure, Back Annotation Calculation	7
VIII	**Testing:** Introduction to Digital Testing - Fault modeling - Fault Simulation - Testing for Single stuck faults - Design For Testability (DFT) - Ad-Hoc DFT - Scan based designs - Built-In Self-Test (BIST)	3

References
1. Neil H. E. Weste, David Harris, Kamran Eshraghian, "Principles of CMOS VLSI Design: A systems perspective", Third Edition, Addison Wesley,2008 2. Majid Sarrafzadeh, C. K. Wong , "An introduction to VLSI physical design", McGraw Hill, 1996, ISBN 0070571945, 9780070571945, 334 pages 3. Khosrow Golshan, "Physical design essentials: an ASIC design implementation perspective", Springer, 2007, ISBN 0387366423, 9780387366425, 211 pages 4. Ban P. Wong, Anurag Mittal, Yu Cao, Greg Starr Contributor Ban P. Wong, Anurag Mittal, Yu Cao, "Nano-CMOS circuit and physical design", John Wiley and Sons, 2004, ISBN 0471466107, 9780471466109

VLS 5235: Wireless Communications and Antenna Design	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome

1. Describe modern wireless and cellular communications.
2. Explain personal and ad-hoc wireless networks.
3. Describe antenna design.

Unit	Topics	No. of Hours
I	**Introduction**: Types of wireless communication, different generations and standards in cellular communication system, satellite communication including GPS, wireless local loop, cordless phone, paging systems, RFID, Cell capacity and reuse, Mobile Radio Propagation	6
II	**Modern wireless technologies**: Multicarrier modulation, OFDM, MIMO system, MIMO-OFDM system, cognitive radio, software defined radio, communication relays, spectrum sharing.	6
III	**Wireless and Cellular Communication**: Multiple Access Schemes: FDMA, TDMA, CDMA and SDMA - Cellular Concept: Frequency Reuse – Channel Assignment – Handoff – Cell Splitting – Cell Sectoring – Micro Zone Method	6

IV	**Wireless personal area networks:** Wireless personal area networks (Bluetooth, UWB and ZigBee), wireless local area networks (IEEE 802.11, network architecture, medium access methods, WLAN standards), wireless metropolitan area networks (WiMAX).	6
V	**Ad-hoc wireless networks**: Design Challenges in Ad-hoc wireless networks, concept of cross layer design, security in wireless networks, energy constrained networks. MANET and WSN. Wireless system protocols, mobile network layer protocol, mobile transport layer protocol, support for mobility.	4
VI	**Antenna design**: Introduction to Antennas, Fundamental parameters of antenna, Antennas for Various Applications, Dipole, Monopole, Loop and Slot Antennas, Linear and Planar Arrays, Microstrip Antennas, Helical Antennas, Horn Antennas, Reflector Antennas	8

References

1. Andrea Goldsmith, "Wireless Communications", Cambridge University Press, 2005.
2. Sanjay Kumar, "Wireless Communication the Fundamental and Advanced Concepts" River Publishers, Denmark, 2015 (Indian reprint).
3. Vijay K Garg, "Wireless Communications and Networks", Morgan Kaufmann Publishers an Imprint of Elsevier, USA 2009 (Indian reprint)
4. J. Schiller, "Mobile Communication" 2/e, Pearson Education, 2012.
5. Iti Saha Misra, "Wireless Communication and Networks: 3G and Beyond", 2/e, McGraw Hill Education (india) Private Ltd, New Delhi, 2013.
6. C.A. Balanis, Antenna Theory – Analysis and Design, John Wiley, 2005
7. J.D. Kraus and R.J. Marhefka, Antennas, McGraw Hill, 2003

ENP 5230: Entrepreneurship	**L**	**T**	**P**	**C**	**Total hours**
	3	**0**	**0**	**3**	**36**

Course Outcome

1. Explain the importance of entrepreneurship and entrepreneurial development model, social responsibilities of business
2. Describe Entrepreneurial Traits and Factors affecting Entrepreneurship process

3. Discuss Business Start-up Process
4. Summarize a business and marketing plan for entrepreneurs.

Unit	Topics	No. of Hours
I	**Introduction to Entrepreneurship:** Meaning and Definition of Entrepreneurship-Employment vs Entrepreneurship, Theories of Entrepreneurship, approach to entrepreneurship, Entrepreneurs VS Manager	6
II	**Entrepreneurial Traits:** Personality of an entrepreneur, Types of Entrepreneurs	5
III	**Process of Entrepreneurship:** Factors affecting Entrepreneurship process	6
IV	**Business Start-up Process:** Idea Generation, Scanning the Environment, Macro and Micro analysis	7
V	**Business Plan writing:** Points to be considered, Model Business plan	6
VI	**Case studies:** Indian and International Entrepreneurship	6

References

1. NVR Naidu and T. Krishna Rao, "Management and Entrepreneurship", IK International Publishing House Pvt. Ltd 2008.
2. Mohanthy Sangram Keshari, "Fundamentals of Entrepreneurship", PHI Publications, 2005

ESD 5232: IT Project Management	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome

1. Illustrate the importance of project planning.
2. Discuss and demonstrate various tools applicable for different phases of the software project.
3. Illustrate the importance of Change management.

4. Illustrate the importance of team work and demonstrate the usefulness of tools in effective handling of the project.
5. Compare the problems in projects that don't follow the process and discuss new trends in software life cycle.

Unit	Topics	No. of Hours
I	**Software Project Planning:** Understand the Project Needs, Create the Project Plan, Diagnosing Project Planning Problems	3
II	**Estimation:** Elements of a Successful Estimate, Wideband Delphi Estimation, Other Estimation Techniques, Diagnosing Estimation Problems.	3
III	**Project Schedules:** Building the Project Schedule, Managing Multiple Projects, Use the Schedule to Manage Commitments, Diagnosing Scheduling Problems.	3
IV	**Reviews:** Inspections, Deskchecks, Walkthroughs, Code Reviews, Pair Programming, Use Inspections to Manage Commitments, Diagnosing Review Problems.	4
V	**Software Requirements:** Requirements Elicitation, Use Cases, Software Requirements Specification, Change Control, Introduce Software Requirements Carefully, Diagnosing Software Requirements Problems	4
VI	**Design and Programming:** Review the Design, Version Control with Subversion, Refactoring, Unit Testing, Use Automation, Be Careful with Existing Projects, Diagnosing Design and Programming Problems	4
VII	**Software Testing:** Test Plans and Test Cases, Test Execution, Defect Tracking and Triage, Test Environment and Performance Testing, Smoke Tests, Test Automation, Postmortem Reports, Using Software Testing Effectively, Diagnosing Software Testing Problems	4
VIII	**Understanding Change:** Why Change Fails, How to Make Change Succeed	3
IX	**Management and Leadership:**	2

	Take Responsibility, Do Everything Out in the Open, Manage the Organization, Manage Your Team	
X	**Managing an Outsourced Project:** Prevent Major Sources of Project Failure, Management Issues in Outsourced Projects, Collaborate with the Vendor	3
XI	**Process Improvement:** Life Without a Software Process, Software Process Improvement, Moving Forward	3

References

1. "Applied Software Project Management", Jennifer Greene, Andrew Stellman (O'Reilly Publications), 2005.
2. "The Art of Project Management", Scott Berkun (O'Reilly Publications), 2005.

ESD 5236: System Software	L	T	P	C	Total hours
	3	0	0	3	36

Course Outcome

1. Designing Assemblers, Loaders, linkers and Compilers.
2. Distinguish context free grammars and parsers
3. Describe intermediate code and code optimization techniques

Unit	Topics	No. of Hours
I	**Assemblers:** Designing one pass and two pass assemblers, Macro-processors.	**5**
II	**Loaders and linkers:** Static linking, Dynamic Linking.	**2**
III	**Compilers:** Lexical Analyzers- Regular Expressions, Finite State Machines – NFA, DFA - Obtaining DFA from regular expressions, Designing lexical analyzers .	**10**
IV	**Context Free Grammars:**	**9**

	Languages, Grammars, Ambiguity, Parse Trees- Parsing, top-down parsing, bottom-up parsing ideas, Recursive Descent Parsing: Removing left recursion. Designing recursive descent parsers, Predictive Parsing: LL(1) grammars .	
V	**Bottom-up Parsing with LR(k) parsers:** Handles, viable prefixes, shift/reduce parsing, LR(0) items, SLR(1) parser and its limitations, LR(1) parser .	**4**
VI	**Intermediate Code:** Parse Trees, Three address codes, Quadruples and triples.	**2**
VII	**Introduction to code optimization:** Principle sources of optimization, Introduction to dataflow analysis.	**4**

References

1. "Principles Of Compiler Design", Aho, Sethi and Ullman
2. "Principle Of Compiler Design", Aho and Ullman
3. "Compiler Construction In C", Alan Holub
4. "System Software", Dhamdhere

VLS 5251: Advanced VLSI Design Lab	**L**	**T**	**P**	**C**	**Total hours**
	0	**0**	**3**	**1**	**36**

Course Outcome

1. Design and simulate various analog VLSI building blocks.
2. Design and simulate mixed signal circuits – ADCs and DACs.

Unit	**Topics**	**No. of Hours**
I	Design and simulate current sources, sinks and references	9
II	Design and simulate various amplifier configurations	15
III	Experiment with nonlinear and dynamic analog circuits	7
IV	Design and analyse various data converter architectures	5

References
1. "CMOS Circuit Design, Layout, and Simulation", Baker, Li, & Boyce, IEEE Press, 1998. 2. "Design of Analog CMOS Integrated Circuits", Razavi, McGraw-Hill, Inc., 2000. 3. "Analog Integrated Circuit Design", Johns & Martin, John Wiley & Sons, 1997. 4. "CMOS Analog Design, 2nd Ed.", Allen & Holberg, Oxford Univ. Press, 1987. 5. "Analysis and Design of Analog Integrated Circuit", Gray & Meyer, John Wiley & Sons, 1984. 6. "Analog VLSI", Mohammed Ismail, & Terri Fiez, McGraw-Hill, Inc. 7. "VLSI - Design Techniques for Analog and Digital Circuits", Geiger, Allen, & Strader, McGraw-Hill, Inc., 8. Cadence user manual

VLS 5252: Low Power VLSI Design Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Experiment static and dynamic power components.
2. Implement static power reduction techniques.
3. Apply dynamic power reduction techniques.

Unit	Topics	No. of Hours
I	Power dissipation in CMOS: Dynamic and Static power components, dynamic power components	9
II	Static power reduction techniques for low power	15
III	Dynamic power reduction techniques for low power	12

References

1. "Low-Power CMOS VLSI Circuit Design",Kaushik Roy and Sharat C. Prasad, Wiley-Interscience.
2. "CMOS Low Power Digital Design", A. Chandrakasan & R. Brodersen, Kluwer Academic Pubs. 1995.
3. "Low Power Design Methodologies",J. Rabaey & M. Pedram, , Kluwer Academic Pubs. 1996.

4. "Low – Power Digital VLSI Design, Circuits and Systems", Bellaour & M.I. Elamstry ,Kluwer Academic Publishers, 1996.
5. S. Imam & M. Pedram, Kluwer Academic Publishers, 1998.
6. "Logic synthesis for Low – power VLSI Designs", B.G.K.Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998.

VLS 5253: Scripting for VLSI Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Experiment shell script programmatically using different features and debugging the code.
2. Operate SED & AWK commands to do more complex task in easy way.
3. Experiment PERL scripts that create and change scalar, array and hash variables.

Unit	Topics	No. of Hours
I	Introduction	6
II	Shell Programming	6
III	Power Tools	9
IV	Perl	15

References

1. "Introduction to Linux – A Beginner's Guide", Machtelt Garrels
2. *"Unix shell programming", Stephen G. Kochan, Patrick H. Wood*
3. *"Sed & awk ",Dale Dougherty, Arnold Robbins*
4. *"Programming Perl", Larry Wall, Tom Christiansen, Jon Orwant*

VLS 5254: Universal Verification Methodology Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Understand the features and capabilities of the UVM class library for SystemVerilog.
2. Create and configure reusable, scalable, and robust UVM Verification Components (UVCs).
3. Combine multiple UVCs into a complete verification environment.

Unit	Topics	No. of Hours
I	UVM Methodology, Stimulus Modeling, Test and Testbench Classes	12
II	UVM component classes, Configuration, UVM Sequences, Connecting to a DUT	12
III	Interface and Module UVCs, Building a Scoreboard, Register Modeling	12

References

1. Vanessa R. Cooper, “Getting started with UVM: A beginner’s guide”, Verilab publisher, 2013.
2. SystemVerilog 3.1a Language Reference Manual

VLS 5281: Advanced Logic Synthesis Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Convert behavioral level logic hardware description language into register transfer logic.
2. Apply constraints and synthesize the combinational and sequential digital circuits.
3. Analyze the area, power, and performance reports.

Unit	Topics	No. of Hours
I	Write register transfer logic level code for combinational and sequential digital systems	9
II	Perform logic synthesis of combinational and sequential circuit description in register transfer logic	18

III	Generate the synthesized netlist and analyse critical path delay, area, power, and performance of the digital system	9

References

1. IEEE Standard for Verilog® Hardware Description Language by IEEE Computer Society
2. Cadence manual for synthesis tool

VLS 5282: Formal Methods Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Apply equivalence checking on digital systems.
2. Apply Model checking on digital systems.
3. Analyze formal verification on clock domain crossing digital systems.

Unit	Topics	No. of Hours
I	Experiment with computer aided design tools for equivalence checking to check register transfer logic level and gate-level descriptions of a design represent the same design	12
II	Experiment with computer aided design tools for model-checking formal verification with user-generated assertions	15
III	Analyse formal verification techniques for the digital systems with clock domain crossing	9

References

1. Logic in Computer Science: Modeling and Reasoning about Systems, Second edition, Michael Huth and Mark Ryan, Cambridge University Press.
2. Principles of Model Checking, Christel Baier and Joost-Pieter Katoen, MIT Press.
3. Model Checking, Edmund M. Clarke Jr., Orna Grumberg, and Doron A. Peled, MIT Press.
4. Cadence user manual for logic equivalence and formal verification

VLS 5283: Machine Learning for VLSI Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Identify the software and tools for designing machine learning applications.
2. Apply concept learning and hypothesis space.
3. Demonstrate Artificial Neural Network, Clustering, Support Vector Machine, Deep Neural Network and Reinforcement Learning models, Support Vector Machine.

Unit	Topics	No. of Hours
I	Goals and applications of machine learning, Basic design issues and approaches to machine learning, Concept learning as search through a hypothesis space, General-to-specific ordering of hypotheses.	12
II	Probability theory and Bayes rule, Naive Bayes learning algorithm - Parameter smoothing, Logistic regression, Bayes nets and Markov nets for representing dependencies, Neurons and biological motivation, Activation functions and threshold units, Supervised and unsupervised learning, Perceptron Model: representational limitation and gradient descent training, Multilayer networks and back propagation, Overfitting.	12
III	Learning from unclassified data, Clustering. Hierarchical Aglomerative Clustering, Non-Hierarchical Clustering - k-means partitional clustering, Expectation maximization (EM) for soft clustering, Semi-supervised learning with EM using labeled and unlabled data, Maximum margin linear separators, Quadractic programming solution to finding maximum margin separators, Kernels for learning non-linear functions, Varying length pattern classification using SVM	12

References

1. Machine Learning, T. Mitchell, McGraw-Hill, 1997
2. Machine Learning, E. Alpaydin, MIT Press, 2010
3. Machine Learning for Big Data, Jason Bell, Wiley Big Data Series

VLS 5284: Physical Design Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Constraint and synthesize the combinational and sequential digital circuits.

2. Design and implement the netlist using floorplan, placement, clock tree synthesis and routing steps.
3. Analyze the area, power, and performance reports.

Unit	Topics	No. of Hours
I	Perform logic synthesis of combinational and sequential circuit description in RTL: Ripple Carry, Carry Look-Ahead, Latch, Flip-flops, counters, FSMs	15
II	Perform physical design flow: Use floorplan, placement, clock tree synthesis and routing	15
III	Back annotation: Extract resistance, capacitance, inductance and simulate the design. Generate and analyse area, power, and performance reports	6

References

1. Cadence manual for synthesis and physical design tool

VLS 5285: Wireless Communication and Antenna Design Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Describe Matlab for wireless communication.
2. Apply Matlab for digital modulation and modulation domain analysis.
3. Examine effects of filters and channel impact in wireless communication.

Unit	Topics	No. of Hours
I	Introduction to Matlab Toolbox and Simulink Introduction to RF system-level simulation of wireless transceivers:	6
II	Apply Model and Simulate for Wireless Systems, Use Matlab tools to design and implement wireless transceivers, Examine simulation for correctness of wireless transceivers	18
III	Design of Zigbee receiver: Use Matlab tools to implement Zigbee receiver, Examine simulation for correctness receivers	12

References

1. Garg, V., 2010. Wireless communications & networking. Elsevier.
2. Cho, Y.S., Kim, J., Yang, W.Y. and Kang, C.G., 2010. MIMO-OFDM wireless communications with MATLAB. John Wiley & Sons.

ENP 5280: Entrepreneurship Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Study of prominence of entrepreneurship.
2. Develop use cases for building a business.
3. Evaluation of factors influencing business venture.

Unit	Topics	No. of Hours
I	Study of use cases for need and prominence of entrepreneurship, associated decision making process.	6
II	Study of report by the National Knowledge Commission on the importance of entrepreneurship in economic development.	6
III	Develop use cases for identifying and evaluating opportunities, developing business plan, assessment of resources, project appraisal and feasibility plan.	9
IV	creating and starting venture includes legal requirements, marketing strategies, financial plans and human resources management	9
V	Design a Case studies of Indian and International Entrepreneurship.	6

References

1. Management and Entrepreneurship, NVR Naidu and T. Krishna Rao, IK International Publishing House Pvt.Ltd, 2008.
2. Fundamentals of Entrepreneurship, Mohanthy Sangram Keshari, PHI Learning Pvt. Ltd., 2005.

ESD 5282: IT Project Management Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Identify the skills and techniques required for project life cycle.
2. Illustrate essential principles associated with project management and their application in business environment.
3. Outline commonly available project management tools.

Unit	Topics	No. of Hours
I	Software project management and its need, evaluation techniques, Project cost estimation techniques.	12
II	Activity scheduling techniques, cost monitoring, contract management and its necessity risk analysis.	12
III	Software quality enhancement techniques, people management in software environment and project team structure.	12

References

1. "Applied Software Project Management", Jennifer Greene, Andrew Stellman (O'Reilly Publications), 2005.
2. "The Art of Project Management", Scott Berkun (O'Reilly Publications), 2005.

ESD 5286: System Software Lab	L	T	P	C	Total hours
	0	0	3	1	36

Course Outcome

1. Design programs for assembler, loader & linker, and compilers
2. Design programs for context free grammars and parsers
3. Design programs for intermediate code and code optimization techniques

Unit	Topics	No. of Hours

I	**Assembler, Loader & Linker, and Compilers**: one pass and two pass assemblers, Static linking, Dynamic Linking, Lexical Analyzers- Regular Expressions, Finite State Machines – NFA, DFA - Obtaining DFA from regular expressions, Designing lexical analyzers	15
II	**Context Free Grammars and Parsers:** Parse Trees- Parsing, top-down parsing, bottom-up parsing ideas, Recursive Descent Parsing: Removing left recursion. Designing recursive descent parsers, Predictive Parsing: LL(1) grammars	15
III	**Intermediate code and code optimization techniques:** Three address codes, Quadruples and triples, dataflow analysis	6
References		
1. Principle of Compiler Design by Aho and Ullman 2. Compiler Construction in C by Alan Holub		

MPT 5200 Mini project - II	**L**	**T**	**P**	**C**	**Total hours**
	0	**0**	**0**	**4**	**48**

Course Outcome

1. Identify the real-world and social relevant problems and perform feasibility analysis for finding solutions.
2. Develop solutions to the identified problems by applying research methodology and development life cycle with appropriate documentation by incorporating ethical standards.
3. Work effectively as a member in a team and communicate technical information effectively.

Unit	**Topics**	**No. of Hours**
I	Problem identification, literature survey, formation of detailed specifications.	48
II	Design and implementation of the proposed system architecture.	
III	Demonstrate an ability to present and defend project work carried out to a panel of experts.	
References		

1. Research articles and Online Resources.

PSD 5200: Professional Skill Development - II	L	T	P	C	Total hours
	0	0	0	1	12

Course Outcome

1. Develop the skills needed for approaching technical and HR interviews.
2. Use mathematical, reasoning, and domain specific skills to solve objective questionnaires in time.
3. Demonstrate depth of knowledge in the chosen field of study.

Unit	Topics	No. of Hours
I	Peer interviews, mock interviews.	12
II	Logical reasoning, mathematical aptitude, domain specific problem solving skills.	
III	Conduction of domain specific knowledge test.	

References

1. R S Aggarwal. Quantitative Aptitude for Competitive Examinations. S Chand, 2017.
2. McDowell, Gayle Laakmann. Cracking the coding interview: 189 programming questions and solutions. CareerCup, LLC, 2015.
3. Domain specific tools and online resources.

VLS 6098: Project Work	L	T	P	C	Total hours
	0	0	0	25	300

Course Outcome

1. Undertake innovative industry/research oriented projects and perform feasibility analysis for finding solutions.
2. Implement and test the proposed design using appropriate framework, programming language and tools.
3. Demonstrate an ability to present and defend project work carried out to a panel of experts.

Unit	Topics	No. of Hours
I	Problem identification, literature survey, formation of detailed requirement specification document.	300
II	Design and implementation of the proposed modules with specific test cases.	
III	Detailed report of the work carried out, present, and defend the project work carried out to a panel of experts.	

References

1. Research articles, domain specific tools and online resources.

Program Outcome and Course Outcome Mapping

Sl. No.	Course Code	Course Name	Credits	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
1	VLS 5001	High Level Digital Design	3	*	*	*		*						
2	VLS 5101	Data Structures	3	*	*	*						*		
3	VLS 5102	Digital Systems & VLSI Design	3	*	*	*		*				*		
4	VLS 5103	Verification	3	*	*	*		*			*			
5	VLS 5131	CAD for VLSI	3	*	*	*		*						
	VLS 5132	System on chip Design	3	*	*	*		*	*					
	ESD 5001	Digital Signal Processing	3	*	*	*		*						
6	VLS 5051	High Level Digital Design Lab	1	*	*	*		*						
7	VLS 5151	Data Structures Lab	1	*	*	*						*		
8	VLS 5152	Digital Systems & VLSI Design Lab	1	*	*	*		*				*		
9	VLS 5153	Verification Lab	1	*	*	*		*			*			
10	VLS 5181	CAD for VLSI Lab	1	*	*	*		*						
	VLS 5182	System on chip Design Lab	1	*	*	*		*	*					
	ESD 5051	Digital Signal Processing Lab	1	*	*	*		*						
11	MPT 5100	Mini Project - 1	4				*	*	*	*	*		*	*
12	PSD 5100	Professional Skill Development – I	1	*							*	*		*
13	VLS 5201	Advanced VLSI Design	3	*	*	*	*	*						
14	VLS 5202	Low Power VLSI Design	3	*	*	*	*	*						
15	VLS 5203	Scripting for VLSI	3	*	*	*								
16	VLS 5204	Universal Verification Methodology	3	*	*	*		*			*			
17	VLS 5231	Advanced Logic Synthesis	3	*	*	*	*							
	VLS 5232	Formal Methods	3	*	*	*		*			*			
	VLS 5233	Machine learning for VLSI Design	3	*	*	*	*		*					

	VLS 5234	Physical Design	3	*	*	*		*						
	VLS 5235	Wireless Communications and Antenna Design	3	*	*	*								
	ENP 5230	Entrepreneurship	3	*		*			*	*	*		*	*
	ESD 5232	IT Project Management	3	*		*		*		*	*	*		
	ESD 5236	System Software	3	*	*	*								
18	VLS 5251	Advanced VLSI Design Lab	1	*	*	*	*	*						
19	VLS 5252	Low Power VLSI Design Lab	1	*	*	*	*	*						
20	VLS 5253	Scripting for VLSI Lab	1	*	*	*								
21	VLS 5254	Universal Verification Methodology Lab	1	*	*	*		*			*			
22	VLS 5281	Advanced Logic Synthesis Lab	1	*	*	*		*			*			
	VLS 5282	Formal Methods Lab	1	*	*	*	*		*					
	VLS 5283	Machine Learning for VLSI Design Lab	1	*	*	*		*						
	VLS 5284	Physical Design Lab	1	*	*	*								
	VLS 5285	Wireless Communications and Antenna Design Lab	1	*		*			*	*	*		*	*
	ENP 5280	Entrepreneurship Lab	1	*		*		*		*	*	*		
	ESD 5282	IT Project Management Lab	1	*	*	*								
	ESD 5286	System Software Lab	1	*	*	*		*			*			
23	MPT 5200	Mini Project - II	4				*	*	*	*	*		*	*
24	PSD 5200	Professional Skill Development - II	1	*							*	*		*
25	VLS 6098	Project Work	25	*	*	*	*	*	*	*	*	*	*	*